FACULTY OF ENGINEERING AND ARCHITECTURE

Design of a high voltage charge pump in advanced CMOS

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Haowei Bi, May 2023

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Design of a high voltage charge pump in advanced CMOS

by

Haowei Bi

Master's dissertation submitted in order to obtain the academic degree of Master of Science in Electrical Engineering

Supervisor: Prof. dr. ir. Guy Torfs, Prof. dr. ir. Johan Bauwelinck

Counsellor: Xin Wang & Achim Vandierendonck

Faculty of Engineering and Architecture

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Abstract - With the increasing demand for high voltage in electronic systems, such as sensor systems, communication devices like RF amplifiers and power amplifiers, as well as MEMS systems, the need for chip-level high-voltage design that is compact and efficient has become essential. This paper presents the design of charge pump circuits to achieve a high voltage of 20 V from a 1.8 V voltage supply for chip-level applications. Given the high integration requirements, the primary focus is to minimize the area and enhance power efficiency. The main challenge lies in the limitation imposed by the breakdown voltage of MOS transistors. This study investigates the fundamental principles of charge pumps and explores the design parameters, including output voltage, ripple, settling time, and power consumption. Dickson charge pump is designed firstly. To overcome the limitations imposed by threshold voltage in the Dickson charge pump output, a charge pump structure utilizing charge transfer switches is studied. Ultimately, the design achieves an efficiency of 71.15% with a 25-stage charge pump structure, operating at a frequency of 100 kHz and a load current of 1 uA.

Keywords - High voltage on chip, Charge pump, Dickson CP, Dynamic CTS's

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Design of a high voltage charge pump in advanced CMOS

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***Abstract*—With the increasing demand for high voltage in electronic systems, the need for chip-level high-voltage design that is compact and efficient has become essential. This paper presents the design of a charge pump circuit to achieve a high voltage of $20\,\mathrm{V}$ from a $1.8\,\mathrm{V}$ power supply for chip-level applications. This study investigates the fundamental principles of charge pumps and explores the design parameters, including output voltage, ripple, settling time, and power consumption. Starting with the Dickson charge pump, circuits utilizing charge transfer switch(CTS's) are also discussed. Ultimately, the design achieves an efficiency of 71.15% with a 25-stage charge pump, operating at a frequency of $100\,\mathrm{kHz}$ and a load current of $1\,\mathrm{uA}$.**

***Index Terms*—High voltage on chip, Charge pump, Dickson CP, Dynamic CTS's**

I. Introduction

In MEMS systems, high voltage is needed to drive specific variable capacitors for improved linearity and reduced phase noise [1]. Generally, external power supplies, boost Chopper, charge pump can be used for generating high voltage.

Given the need for higher integration density and lower power consumption, both the channel length and supply voltage of CMOS are becoming increasingly smaller.the application of charge pumps has become increasingly widespread.

Section II introduces general design considerations of charge pump. Section III and section IV provide a specific design of the Dickson charge pump and CTS's charge pump. Finally, a comparative analysis is conducted between the two topology structures.

II. Dickson charge pump

In [2], the principle of Dickson charge pump is introduced. Fig. 1 indicates the schematic of a four-stage Dickson charge pump.

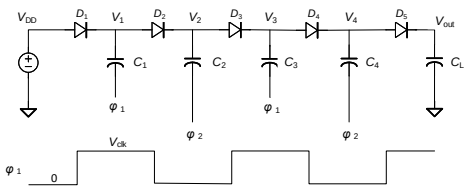

Fig. 1: Schematic of 4-stage Dickson charge pump without loading

When designing a 4-stage charge pump, various factors need to be considered when selecting each component, such as output voltage, ripple, power efficiency, and so on. Each of these factors will be discussed in detail in this section.

A. Output voltage

As charge is transferred from the voltage source in a step-by-step manner, so the voltage increases incrementally before reaching a steady state and increases stage by stage. For a N-stage charge pump, assume MOSFET size limitations on load current and parasitic capacitance are ignored, the output voltage can be expressed as:

$$V_{out} = V_{DD} + N \cdot \Delta V - (N+1) \cdot V_{th} \tag{1}$$

$$\Delta V = V_{clk} \cdot C_i - \frac{I_o}{f \cdot C_i} \tag{2}$$

where V_{clk} is the high voltage of the clock pulse, C_i is the capacitor in each stage, I_o is the loading current and f is the frequency of clock pulse. If the limitation of the MOSFET size is considered, a term related to the load current needs to be subtracted from the expression of ΔV.

B. Ripple

Ripple is generated by the charging and discharging process of C_L due to the period change of clock signals. In pumping time, the output capacitor is charged by the capacitor C_N, so V_{out} goes up. In blocking time, the output capacitor is discharged by the loading current,so the V_{out} goes down. The ripple of the output voltage is given by

$$Rippple = \frac{I_o \cdot \Delta t}{C_L} = \frac{I_o}{2 \cdot f \cdot C_L} \tag{3}$$

where Δt is time of charging or discharging, and C_L is the output capacitor .

C. Power consumption

For a realistic charge pump circuit, power current consists of the current consumption in a ideal charge pump at steady stage and power current due to parasitic effects. The ratio of output power over input power is used to calculated the power efficiency:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_o}{V_{DD} \cdot I_{in} + V_{clk} \cdot I_b} \tag{4}$$

where I_b is the current flowing through buffer.

III. Design of Dickson charge pump

A. Switch design

Transistor with smaller channel length experiences worse short channel effect and gives larger leakage current, resulting in a larger voltage drop at the output of the switch. Therefore, it is necessary to increase the channel length. Taking into account the trade-off between area and output voltage, ultimately, a channel length value of $6\,\mathrm{um}$ is chosen.

For designing the channel width, when a $1\,\mathrm{uA}$ loading current is added, the voltage between gate terminal and source terminal V_{GS} is large when size of transistor is small, which leads to incompletely charging of V_1. Considering that increasing the transistor size results in larger occupied area, the W/L value of $40.3\,\mathrm{um}$ / $6\,\mathrm{um}$ is chosen.

B. Area limitation

In the design of a charge pump, the area occupied by the circuit is also an important consideration. For a $60\,\mathrm{pF}$ capacitor, it occupies an area of $10\,706\,\mathrm{um}^2$ with a capacitance density denoted as $5.604\,\mathrm{fF}/\mathrm{um}^2$, which is much larger than the total area of transistor and buffer $1127.902\,\mathrm{um}^2$. So the area of circuit can be approximated as the area of capacitors:

$$Area = (NC_i + C_L) \cdot C_{density} \tag{5}$$

C. Capacitance size choice

a) Capacitance in each stage

The selection of capacitance value is primarily considered from two aspects: area and efficiency.

Small value of C_i means more stages and large value of C_i means larger area for each stage. The optimal value of capacitance is $15\,\mathrm{pF}$, occupying an area of 203 $0.203\,\mathrm{mm}^2$.

For efficiency, small capacitance leads to small output voltage according to Equation 1 and Equation 2, which cause small efficiency. While capacitance reaches a certain value, continuing to increase capacitance will not significantly increase V_{out}, so the efficiency is almost unchanged when the capacitance is large. As can be seen in Fig. 2 that When

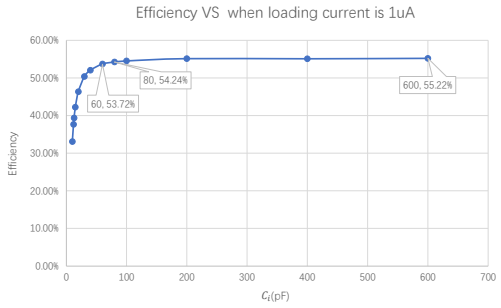

Fig. 2: Efficiency VS C_i when I_o is 1 μ A

the capacitance is $60\,\mathrm{pF}$, the efficiency is 53.72%, which has almost reached its maximum value for the given load. Therefore, when the load is $1\,\mathrm{uA}$, considering both power efficiency and area, the optimal value for the capacitance is chosen as $60\,\mathrm{pF}$.

b) Output capacitance

The output capacitor C_L is related to ripple. When frequency is fixed, C_L is inversely proportional to the ripple. When loading current is $1\,\mathrm{uA}$ and frequency is at $200\,\mathrm{kHz}$, an output capacitor of $100\,\mathrm{pF}$ is selected. At this time, the ripple is $25\,\mathrm{mV}$, which is 1.25% of the output voltage.

D. Frequency choice

Frequency affects efficiency, output voltage ripple, and output current of the circuit. The efficiency of the charge pump increases with increasing frequency because more charge is transferred per unit time. However, When the frequency increases to a certain value, increasing the frequency will decrease efficiency as the buffer power consumption increases. Frequency at $200\,\mathrm{kHz}$ is considered as the optimal frequencies, with a efficiency of 53.72%.

E. Power efficiency optimization

With increasing the loading current while change the frequency to keep ripple constant, V_{out} will decrease as I_o increases, shown in Fig. 3, because of the MOSFET size limitations on load current. According to Equation 6, the power efficiency will decrease following the decrease of V_{out}. Equation 6 is derived by apart the buffer power into two

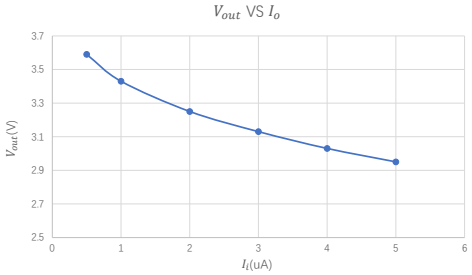

Fig. 3: V_{out} VS I_o

parts: one part related to the loading current and another part consumed by the parasitic capacitance.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_o}{V_{DD} \cdot I_{in} + N \cdot V_{clk} \cdot I_o + C_b \cdot f \cdot V_{clk}^2} \tag{6}$$

where C_b is the parasitic capacitance in buffer,I_{in} is the input current, which is equal to I_o.

When frequency is fixed and ripple is changed, as V_{out} can be expressed by I_o according to Equation 1 and Equation 2. Combine with Equation 6, there will be optimal value of I_o. From simulation results, the optimal I_o is $2\,\mathrm{uA}$, with an efficiency of 56.07%.

IV. Charge pump with Charge transfer switches(CTS's)

Dickson charge pump has a drawback of V_{th} loss. In [3] new topology utilizing charge transfer switches is applied, classified into static CTS's and dynamic CTS's. For static CTS's, parallel MOSFET switches are applied to MOSFET

diodes. But as the MOSFET switches is closed all the time, static CTS's has a problem of reverse charge sharing. To solve this problem, inverters are used to control these switches in dynamic CTS's. The schematic of dynamic CTS's charge pump is shown in Fig. 4.

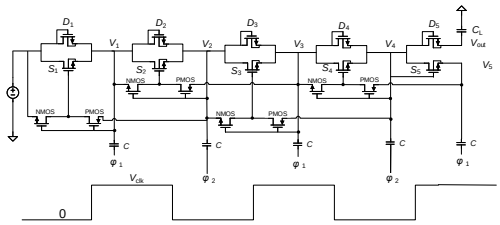

Fig. 4: Schematic of dynamic CTS's charge pump

A. MOSFET design

For the design of MOSFET diodes(MD) and switches(MS), same considerations are taken into account as in Dickson charge pump. For the inverter, driving capability of NMOS should be strong to reduce the reverse charging sharing time. And driving capability of PMOS should not be too strong to weak NMOS relatively. The parameters are shown in Table I:

W/L of MD	W/L of MS	W/L of NMOS	W/L of PMOS
20 um/ 8 um	2 um/ 6 um	8 um/ 200 nm	1.335 um/ 8 um

TABLE I: MOSFETs size in Dynamic CTS's

B. Capacitance size and frequency choice

The design of capacitors and frequency is similar to the situation in Dickson charge pump. The optimal value of the capacitor is $100\,\mathrm{pF}$.And the optimal frequency is chosen as $100\,\mathrm{kHz}$. For C_L, to maintain a ripple of $25\,\mathrm{mV}$, the chosen value is $200\,\mathrm{pF}$.

C. Power efficiency optimization

Efficiency varies with loading current and the maximum efficiency can reach 67% when the load is $3\,\mathrm{uA}$, whereas the efficiency drops to only 35% when the load is $15\,\mathrm{uA}$.

V. Conclusion

In this thesis, how to generate on-chip high voltage on CMOS device is designed. The objective of this article is to achieve a 20V output using charge pump from a 1.8V supply voltage while simultaneously reducing chip area and improving power efficiency. Dickson charge pump and dynamic CTS's charge pump are designed.

Fig. 5 depicts a comparison of two scenarios when V_{out} is 20V. One scenario is when the parameters of the Dickson and dynamic CTS's are set the same, while the other scenario is when the Dickson and dynamic CTS's are set to their respective optimal parameters. The load current is fixed at $1\,\mathrm{uA}$.

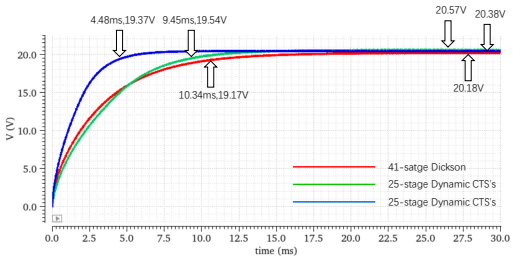

Fig. 5: Comparison of three situations

When all the parameters in Dickson charge pump and dynamic CTS's are same, the dynamic CTS's structure can use a smaller size of $0.285mm^2$ and provide a high power efficiency of 53% to reach the same output voltage of 20V. Also has a lower settling time of 4.48 ms to achieve 95% of 20V. For the respective optimal situation, although larger capacitance and lower frequency can increase the efficiency, more area is required. So design which kind of charge pump is a trade-off between the area and power efficiency. Table II shows simulation results in detail.

	Dickson	Dynamic CTS's	Dynamic CTS's
Stages	41	25	25
V_{out}	20.18V	20.38V	20.57V
Ripple	25mV	25mV	25mV
Frequency	200kHz	200kHz	100kHz
C_i	60pF	60pF	100pF
C_L	100pF	100pF	200pF
$T_{settling}$	10.34ms	4.48ms	9.45ms
Area	$0.457mm^2$	$0.285mm^2$	$0.482mm^2$
Efficiency	43.33%	53%	71.15%

TABLE II: Parameters in design

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1

Introduction

This chapter covers general conception of high voltage applications, how the high voltage can be generated, The supply voltage and channel length scaling on CMOS technology and the goal of this thesis.

1.1 High voltage application

High voltage, which exceeds the maximum supply voltage of sub-micron CMOS technology, is now being increasingly applied in various electronic systems. In nonvolatile memories like EEPROM and flash memory, high voltage is required for programming or erasing on the chip[1]. In radio frequency identification (RFID) systems, high voltage is needed to drive the memory module in the tag to record product information data[2]. In MEMS systems, variable capacitors (such as MOS or PN junction capacitors) are utilized to enhance the linearity of tunable RF filters[3] or improve the phase noise of voltage-controlled oscillators[4]. However, achieving the desired performance of these variable capacitors often requires high-voltage power supplie[5]. In addition, for measuring the acoustic ringing effect of electro-optic (EO) crystals, a high voltage square pulse with fast response is required. This is essential to accurately analyze and characterize the behavior of the EO crystal under acoustic excitation[6]. Besides, high voltage is applied in nematic liquid-crystal (NLC) devices to rapidly drive the molecular director, reducing the required time for state transitions[7].

1.2 High voltage generation

In the realm of electronic circuit applications, there exists a prevalent need to fulfill high voltage requirements. To address this demand, several commonly employed methods are employed, each designed to achieve the desired voltage levels while adhering to established industry standards and safety protocols. Five methods are discussed below:

External power supplies This way is the most easy way to supply voltage. However, in order for CMOS to withstand high voltages, specific process technologies are required, which can lead to increased costs and limitations on the maximum achievable voltage. For example, one dedicated technology Alcatel Mietec HBIMOS allows CMOS sections to operate up to 15V[8].

Boost Chopper The Boost circuit is based on the principle of utilizing an inductor and a switch element (such as a MOSFET) to periodically switch and interrupt the circuit in order to convert electrical energy. It is commonly used for increasing the output voltage from a lower input voltage level. The Boost circuit is suitable for applications where high output voltage is required, but it is more applicable to scenarios with relatively larger current requirements.

Charge pumps Charge pump is a DC-DC converter that converts low voltage to high voltage. But unlike the common BOOST circuit, the charge pump does not require inductive components, it only consists of switches and capacitors. Each stage is composed of a switch (MOSFET or diode) and a capacitor in series. They are efficient and compact solutions for boosting voltage levels.

Voltage multipliers Voltage multiplier circuits, such as Cockcroft-Walton multipliers[9], can generate higher voltages by using a series of capacitors and diodes to multiply the input voltage. Voltage Multiplier cell can also be integrated with windings to work as a high step-up nonisolated dc–dc converter to achieve high voltage conversion ratio[10].

Transformers A transformer can convert input voltage to a higher voltage through magnetic coupling. By adjusting the turns ratio of the transformer, different output voltages can be achieved.

Applying external voltages imposes higher process requirements and costs. Compared to voltage multipliers and high-voltage integrated circuits (HVICs), charge pumps provide more controllable outputs, which can be adjusted by tuning the frequency, stages, and capacitance values. Furthermore, charge pump circuits consist only of CMOS and capacitors in series, resulting in a simple structure without external components and achieving a higher level of integration. And the most importantly, Charge pumps are widely used for low supply voltage situations.

1.3 The supply voltage and channel length scaling on CMOS technology

Figure 1.1 illustrates the trend of supply voltage V_{DD} and Equivalent Oxide Thickness(EOT) over the past 50 years. As the size of EOT continues to decrease, the voltage drop across the gate oxide layer reduces to improve the reliability of the transistor. On the other hand, the scaling down on voltage brings a power consumption reduction for digital intensive circuit in advanced nano CMOS technology.

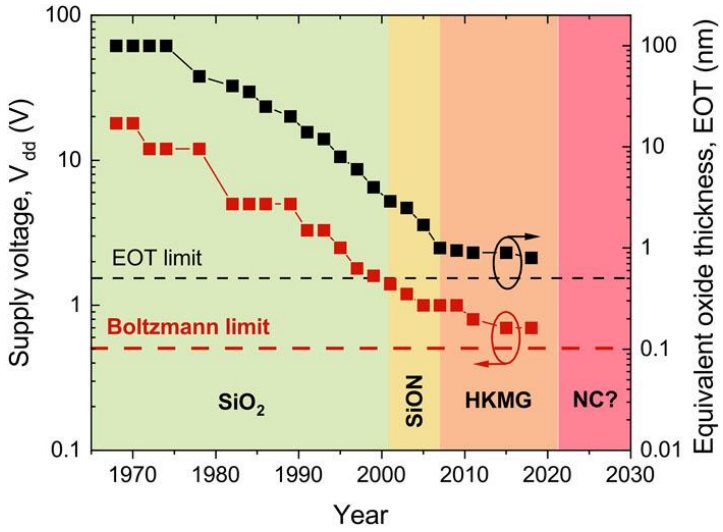

Figure 1.1: Historic trend of supply voltage [11]

Figure 1.2 indicates the historic trend of gate length from 1970 to 2020. In 2009, 28 nm can already be implemented. Gate length has been a critical parameter in driving the advancements in integration technology, playing a pivotal role in improving performance, packing density, power efficiency, and transistor cost. A lower nanometer process technology offers higher integration, lower power consumption, and improved performance. However, smaller gate length poses challenges related to complexity, cost, yield, reliability, design, and timing. In this dissertation, 28 nm CMOS devices are applied.

Figure 1.1 and Figure 1.2 pose three major challenges for a charge pump design. Firstly, the small break down voltage of the transistor requires careful design both in schematic and layout to avoid any potential reliability issue. Secondly, the low available voltage in advanced CMOS technology require more stages to achieve the largest output voltage at the spend of more chip area and higher power consumption. Thirdly, the short channel length addresses a large leakage when a transistor is at 'off' state, ultimately resulting a large area design since minimum channel length choice is impossible.

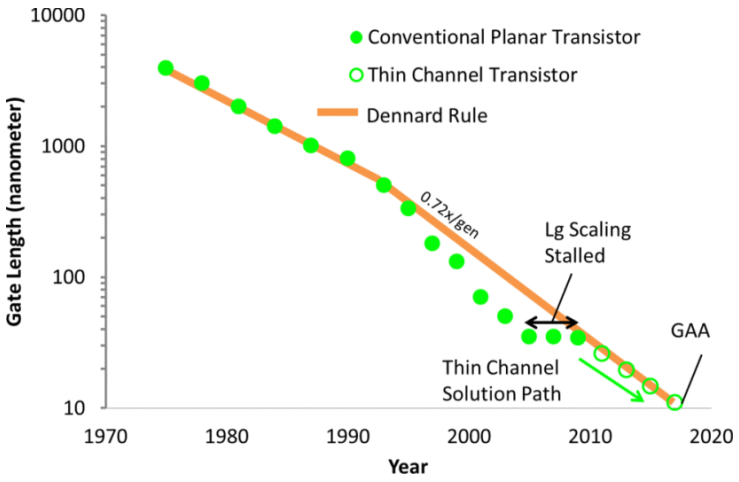

Figure 1.2: Historic trend of gate length [12]

illustrate a clear trend in the field, wherein the pursuit of small area and low power consumption is prominent. To achieve this, the implementation of charge pumps with a simplistic structure, compact area, and high voltage output is becoming increasingly prevalent. By utilizing low DC voltages, such charge pumps offer a viable solution that finds widespread adoption in various applications.

1.4 Goal of this thesis

The objective of this paper is to design a charge pump structure that achieves an output voltage conversion from a 1.8V low-voltage DC power supply to a 20V high-voltage DC output. The analysis focuses on the system's area occupancy and power consumption when applying loading currents. The charge pump structures considered include the Dickson charge pump[13], charge pumps utilizing charge transfer switches (CTS)[1], boost-trap structures[14], series-parallel charge pumps, and charge pumps with adaptive number of stages[15]. This paper primarily focuses on the design, analysis, and comparison of the Dickson charge pump and charge pump structures utilizing CTS.

Chapter 2 introduces the basic principles of the Dickson charge pump and the parameters to consider during its design. Chapter 3 discusses how to design the Dickson charge pump and limitations of Dickson charge pump. Chapter 4 presents the principles and design of two kinds of charge pumps utilizing charge transfer switches,which are static CTS's and dynamic CTS's respectively. And a comparative analysis of the Dickson charge pump and the dynamic CTS charge pump in terms of output, load, area, and power consumption is provided.

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2

Dickson Charge Pump

2.1 The principle of Dickson charge pump

To understand how Dickson charge pump works, consider a 4-stage charge pump shown in Figure 2.1.

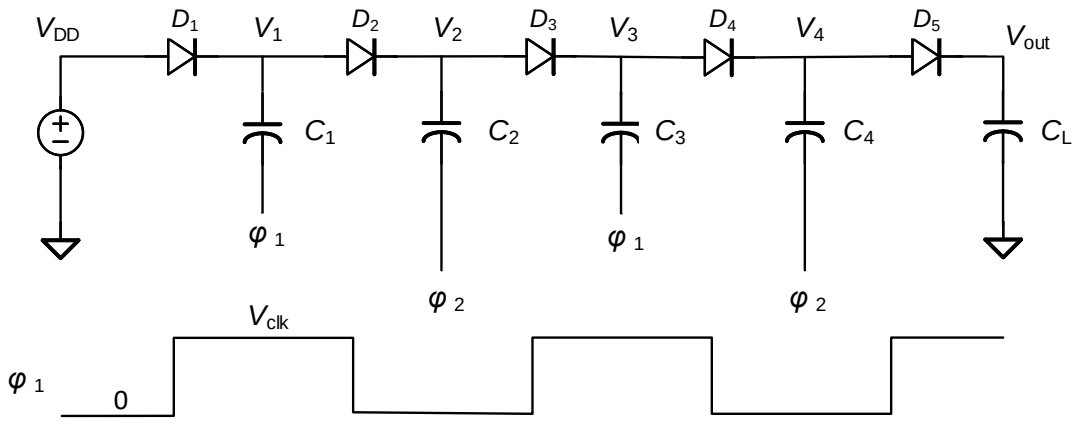


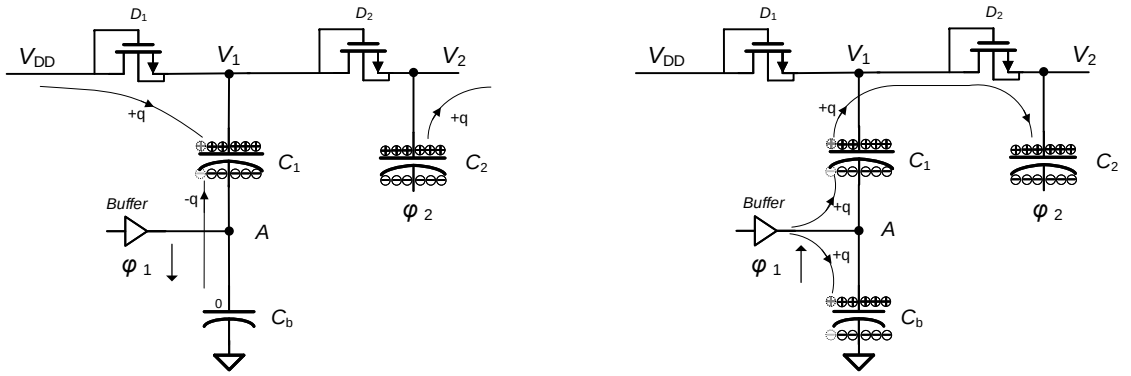
Figure 2.1: Schematic of 4-stage Dickson charge pump without loading

Circuit is supplied by a low DC voltage of 1.8 Volt. V_1 to V_4 refers to nodes voltages. For each stage, diode works as a switch, and a capacitor is used to store and release charges when switch is on and off. One end of the two sides of capacitor is connected to the diode, and the other end is connected to the clock pulse. All the odd-donated stages are controlled by ϕ_1, all even-donated stages are controlled by ϕ_2. The phase difference of ϕ_1 and ϕ_2 is 90 degrees. The state of the switches are controlled by these two out-of-phase clock phases. The output capacitor after the last stage is connected to ground instead of clock signal, acting as a low-pass filter together with the last switch. This filter suppresses the influence of the high-frequency response of the output clock on the output voltage, in other words, output capacitor can reduce the ripple[16].

Figure 2.2 indicates the process of charge transfer in the first stage. The clock voltage flows into the circuit after passing through the buffer, where C_b is the parasitic capacitance on the buffer.

- When ϕ_1 is low, the process is shown in Figure 2.2a. The voltage at point A is 0, and the charge on the upper and lower plates of C_b is 0. At this time, D_1 is turned on, source voltage charges V_1, and the positive charge flows from V_{DD} to V_1. The upper plate of capacitor C_1 experiences an increase in positive charge, resulting in the subsequent flow of negative charge from the ground towards the lower plate of C_1, thereby allowing for the accumulation and storage of charge within C_1.
- When ϕ_1 is high, the positive charge from buffer flows to the lower plate of C_1. The positive charge counteracts the negative charge residing on the lower plate, facilitating the transfer of positive

charge from the upper plate of C_1 through diode D_2 to the next stage. At the same time, the buffer charges the C_b, and the positive charge flows to the upper plate of the C_b. C_b also consumes power, which will be discussed in power consumption section later.



(a) Charge transfer of V_1 when ϕ_1 is low

(b) Charge transfer of V_1 when ϕ_1 is high

Figure 2.2: Charge transfer process in the first stage

The essential reason why the voltage can be increased is that the charge from the power supply charges the capacitance of each stage. The voltage is increased by controlling the charging and discharging process of the capacitor through the two out-of-phase clock signals. The clock signals are used to control the capacitor to store and release the charge to realize the charging and discharging process, and finally realize the step-by-step increase of the voltage. In [17], the recurrence formula of the output voltage V_{out} is derived in detail, by obtaining the total consumed charge in two ways. The first way is to calculate the total charge stored in each capacitor. The second way is to calculate the charge transferred in one time cycle, illustrated in figure 2.3 and 2.4 respectively. For the first method, in a N-stage charge pump, define $Q_{i,j}$ ($1 \leq \mathrm{i} \leq \mathrm{N}$) as charge stored in capacitance at i^{th} stage C_i at time j, and define the total charge consumed by i^{th} stage from initial time 0 to time j as $Q_{DD,i,j}$, which is the sum of charge transferred to C_{i+1}, C_{i+2}, ..., C_N and the output capacitance C_L. ΔQ_i is the increased charge in each stage. The process is shown in figure 2.3[17] .

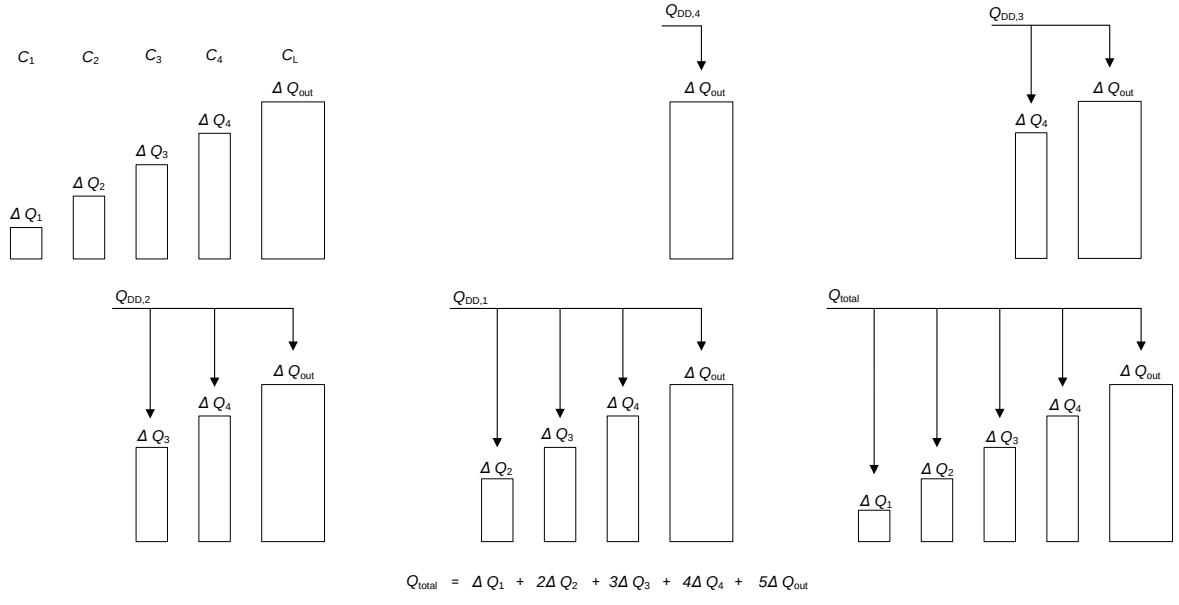


Figure 2.3: The first method to calculate transferred charge

To get recurrence formula of the output voltage, the total consumed charge needs to be calculated. Define Q_{total} as the total charge consumed by the circuits during time j. From Figure 2.3, the charge consumed by the last stage is the charge flowing to the load:

$$Q_{DD,N,j} = Q_{load,j} - Q_{load,0} \tag{2.1}$$

For the i^{th} stage,

$$Q_{DD,i,j} = \sum_{k=i+1}^{N} (Q_{k,j} - Q_{k,0}) + Q_{load,j} - Q_{load,0} \tag{2.2}$$

Then the total charge consumed by the whole charge pump circuits:

$$Q_{total} = \sum_{i=0}^{N} Q_{DD,i,j} = \sum_{i=0}^{N}[\sum_{k=i+1}^{N} (Q_{k,j}-Q_{k,0})+Q_{load,j}-Q_{load,0}] = \sum_{k=1}^{N} k(Q_{k,j}-Q_{k,0})+(N+1)(Q_{load,j}-Q_{load,0}) \tag{2.3}$$

Define *q(j)* as the amount of charge flowing from one capacitor C_i to the next capacitance C_{i+1} at time j in one clock period. Analyze from the first stage. There are several assumptions that need to be satisfied when analyzing.

- Each MOSFET has constant value of threshold voltage V_{th} [18].
- The capacitance in each stage C_i ($1 \leq$ i $\leq$ N)is identical to each other. And the amount of charge transferred to output stage in steady state is identical to the amount of charge transferred from one stage to the next stage.
- Assume the first diode D_1 is off when t=j.
- Parasitic capacitance is not taken into account.

Then expression of the charge stored in C_1 at time j can be written:

$$Q_{1,j} = C_1 \cdot V_{1,j} = C_1 \cdot (V_{DD} - V_{th}) \tag{2.4}$$

V_{th} is the threshold voltage of diodes and V_{DD} is the source voltage. When the first stage is charging the second stage, the amount of charge transferred from C_1 to C_2 is *q(j)*. Then the amount of charge remaining on C_1 is $Q_{1,j}-$ *q(j)*, and the amount of charge remaining on C_2 is $Q_{2,j}+$ *q(j)*. So at time $j+\frac{1}{2}$, the voltages at the first stage and the second stage $V_{1,j+\frac{1}{2}}$ and $V_{2,j+\frac{1}{2}}$ are shown in Equation 2.5 and Equation 2.6 respectively.

$$V_{1,j+\frac{1}{2}} = \frac{Q_{1,j} - q(j)}{C} \tag{2.5}$$

$$V_{2,j+\frac{1}{2}} = \frac{Q_{2,j} + q(j)}{C} \tag{2.6}$$

As the second stage will be charged only when ϕ_1 is high, in stead state (at time $j+\frac{1}{2}$), the maximum voltage that the second stage can reach is limited by the threshold voltage. The following equations can be obtained under the condition that the second diode D_2 is off when $t = j+\frac{1}{2}$:

$$V_{DD} + V_{1,j+\frac{1}{2}} - V_{2,j+\frac{1}{2}} = V_{th} \tag{2.7}$$

Combine Equation 2.5, Equation 2.6 and Equation 2.7, $Q_{2,j}$ can be calculated as :

$$Q_{2,j} = 2C \cdot (V_{DD} - V_{th}) - 2q(j) \tag{2.8}$$

Similarly, the third diode D_3 is off when $t = j$:

$$V_{DD} + \frac{Q_{2,j}}{C} - \frac{Q_{3,j}}{C} = V_{th} \tag{2.9}$$

Combine Equation 2.8 and Equation 2.9, $Q_{3,j}$ can be derived as:

$$Q_{3,j} = 3C \cdot (V_{DD} - V_{th}) - 2q(j) \tag{2.10}$$

Then extend to general expression for N stages.When N is odd,

$$Q_{2k-1,j} = (2k-1) \cdot C \cdot (V_{DD} - V_{th}) - 2(k-1)q(j) \tag{2.11}$$

When N is even,

$$Q_{2k,j} = 2k \cdot C \cdot (V_{DD} - V_{th}) - 2kq(j) \tag{2.12}$$

where $1 \leq \mathrm{k} \leq \frac{N}{2}$. Consider the case where N is even, the charges stored in the last capacitor C_N at time j is

$$Q_{N,j} = (N-1) \cdot C \cdot (V_{DD} - V_{th}) - Nq(j) \tag{2.13}$$

When $t = j$, the output diode D_{N+1} is off, so

$$V_{DD} + \frac{Q_{N,j}}{C} - V_{out} = V_{th} \tag{2.14}$$

Combine Equation 2.13 and Equation 2.14, the amount of charge flowing from one capacitor C_I to the next C_{k+1} q can be expressed as:

$$q(j) = \frac{C}{N}((N+1)(V_{DD} - V_{th} - V_{out}) \tag{2.15}$$

Then the charge stored in each stage is calculated as[18]:

$$Q_{2k-1,j} = \frac{2(k-1)}{N} \cdot C \cdot (V_{out} - (V_{DD} - V_{th})) + C \cdot (V_{DD} - V_{th}) \tag{2.16}$$

$$Q_{2k,j} = \frac{2k}{N} \cdot C \cdot (V_{DD} - V_{th}) \tag{2.17}$$

According to Equation 2.16 and Equation 2.17 , assume the initial condition that: $Q_{2k-1,0} = C(V_{DD} - V_{th})$,$Q_{load,0} = C_{load}(V_{DD} - V_{th})$and $Q_{2k,0} = 0$. Then the total consumed charge can be derived from Equation 2.3 as [17] :

$$Q_{total} = (N+1)C_{out}(V_{out,j} - (V_{DD} - V_{th})) \tag{2.18}$$

$$C_{out} = C_{load} + A(N)C \tag{2.19}$$

$$A(N) = \frac{4N^2 + 3N + 2}{12(N+1)} \tag{2.20}$$

$$A(N) = \frac{4N^2 - N - 3}{12N} \tag{2.21}$$

Equation 2.20 and equation 2.21 correspond to the cases where N is even and odd respectively.

Except for calculated the consumed charge in each stage, calculating the consumed charge in one cycle time is also considered. Figure 2.4 indicates how this method works. Define $q_{DD}(j)$ as the total supplied charge by the source from time j to j+1(during one clock period). Define $q_{total}(j)$ as the total supplied charge by the source from time 0 to time j. As all charges come from the source, $q_{DD,j}$ is expressed as:

$$q_{DD}(j) = (N+1)q(j) \tag{2.22}$$

And the total supplied charge during time 0 to j is described as

$$q_{total}(j) = \sum_{n=0}^{j} q_{DD}(j) = \sum_{n=0}^{j} (N+1)q(j) \tag{2.23}$$

Combine Equation 2.15 and Equation 2.23, the final expression of $q_{total}(j)$ can be written as:

$$q_{total}(j) = (N+1)\sum_{n=0}^{j} \frac{C}{N}[N(V_{DD} - V_{th}) + V_{DD} - V_{th} - V_{out,n}] \tag{2.24}$$

Now the total charge consumed by the circuit has been deduced by two methods, which are presented in Equation 2.18 and Equation 2.24 respectively. Combining these two equations, the following expression can be obtained:

$$C_{out}(V_{out}(j) - (V_{DD} - V_{th})) = \sum_{n=0}^{j} \frac{C}{N}[N(V_{DD} - V_{th}) + V_{DD} - V_{th} - V_{out,n}] \tag{2.25}$$

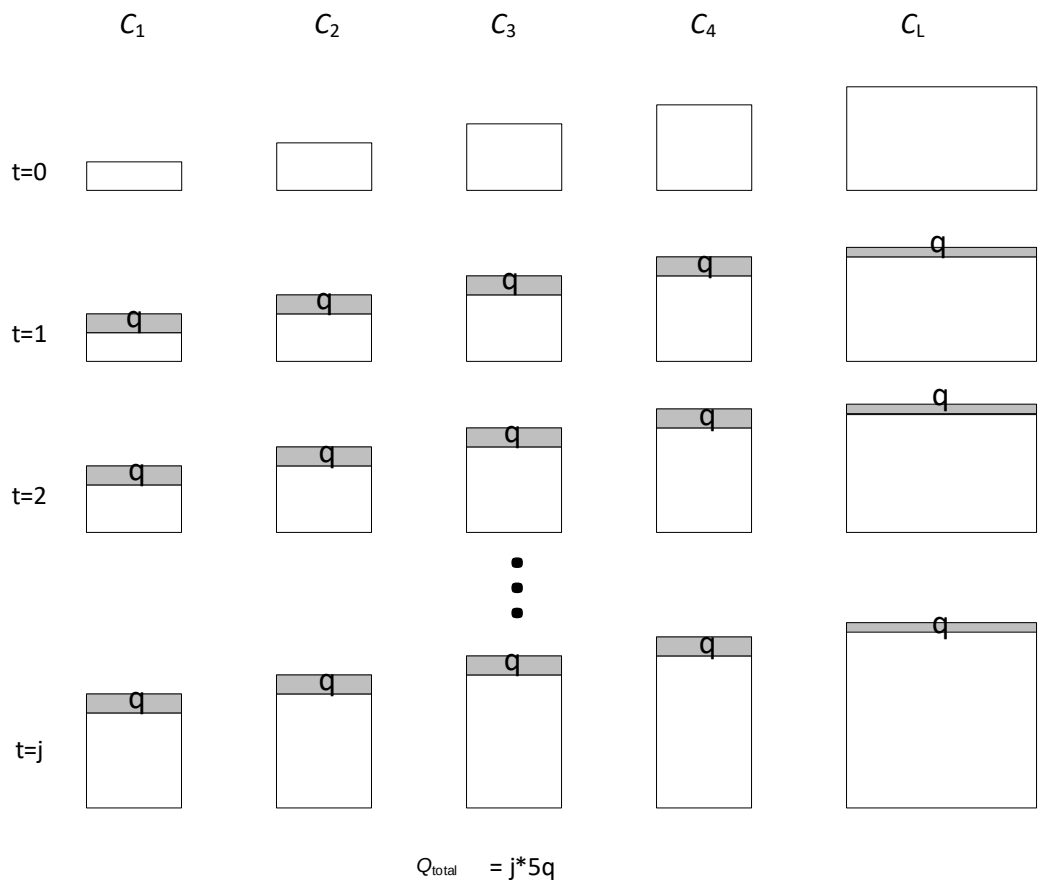


Figure 2.4: The second method to calculate transferred charge

Then the charge deviation from time j to j+1 is

$$C_{out}(V_{out}(j+1) - V_{out}(j)) = \frac{C}{N}[N(V_{DD} - V_{th}) + V_{DD} - V_{th} - V_{out}(j+1)] \tag{2.26}$$

As have been assumed before, the initial output voltage is $V_{DD} - V_{th}$. So the output voltage at time j is calculated:

$$V_{out}(j) = N(V_{DD} - V_{th}) + V_{DD} - v_{th} - N(V_{DD} - V_{th})\beta^j \tag{2.27}$$

$$\beta = 1/(1 + \frac{c}{NC_{out}}) \tag{2.28}$$

2.2 Parameters of Dickson charge pump

2.2.1 Output voltage

Output voltage is an important parameter to take into account. Consider the same 4-stage charge pump shown in Figure 2.1. Analyze the voltage dynamically. Assume all the initial values of node voltage is 0 V, all the diodes are ideal(threshold voltage of the diode is ignored), and the period of the clock driving the charge pump is significantly greater than the time constants associated with the RC circuit, rendering the RC time constant effects negligible. The dynamic processes of voltage changing is shown in Figure 2.5. Analyze from the first stage again.

- At time $t = 0$, ϕ_1 is low, ϕ_2 is high. The first diode D_1 is turned on and the charge flows from the voltage source to the first capacitance C_1 through D_1, so the voltage at node 1 V_1 will be increased to V_{DD}. The second diode D_2 and the forth diode D_4 are turned off, and the voltage at node 2 V_2 and at node 4 V_4 will be increased by the clock pulse to V_{clk}. The third diode D_3 is turned on, and the voltage at node 3 V_3 will be increased to V_{clk} by charges flowing from the capacitance at second stage C_2. Diode at output stage D_5 is turned on so the output voltage V_{out} will be V_{clk}.
- At time $t = T/2$, ϕ_1 goes from low to high, and ϕ_2 goes from high to low. D_1 is turned off and V_1 is increased by the clock pulse to $V_{DD} + V_{clk}$. D_2 is turned on. As ϕ_2 is low, V_2 will be pulled down by the clock immediately. Because V_1 is larger than V_2, V_2 Will be pumped to $V_1 = V_{DD} + V_{clk}$ in a very short time. D_3 is turned off and V_3 is increased by the clock pulse to $V_{DD} + V_{clk}$. D_4 is turned on. The change of V_4 is similar to the process of V_2. V_4 is pumped to $V_3 = V_{DD} + V_{clk}$. D_5 is turned off. The output stage is only charged when the clock of N^{th} stage is high, so V_{out} remains at V_{clk}.
- At time $t = T$, ϕ_1 is low, ϕ_2 is high. V_1 is pulled down by the clock to V_{DD}. V_2 is pulled up by the clock to $V_{DD} + 2 * V_{clk}$. V_3 is pulled down by the clock to V_{DD} and charged by C_2 to $V_{DD} + 2 * V_{clk}$. V_4 is pulled up by the clock to $V_{DD} + 2 * V_{clk}$. As the last diode is closed, the 4^{th} stage will pump the charge to the output stage to increase V_{out} to $V_{DD} + 2 * V_{clk}$.
- At time $t = 3T/2$, ϕ_1 is high, and ϕ_2 is low. V_1 is pulled up to $V_{DD} + V_{clk}$ again.The clock will firstly pull down V_2 to $V_{DD} + V_{clk}$. At this moment, $V_1 = V_2$, so V_2 will be stable at $V_{DD} + V_{clk}$. V_3 is pulled up to $V_{DD} + 3 * V_{clk}$ and V_4 is charged by V_3 to $V_{DD} + 3 * V_{clk}$. V_{out} remains at $V_{DD} + 2 * V_{clk}$ as the last switch is open.
- At time $t = 2T$, ϕ_1 is low, ϕ_2 is high. V_1 is pulled down by the clock to V_{DD}. V_2 is pulled up by the clock to $V_{DD} + 2 * V_{clk}$. The clock will pull down V_3 to $V_{DD} + 2 * V_{clk}$. Since V_2 and V_3 have the same value, V_3 will not be charged. So V_3 remains at $V_{DD} + 2 * V_{clk}$. V_4 is pulled up by the clock to $V_{DD} + 4 * V_{clk}$. And V_{out} is charged to $V_{DD} + 4 * V_{clk}$.
- At time $t = 5T/2$, ϕ_1 is high, and ϕ_2 is low. V_1 is pulled up to $V_{DD} + V_{clk}$. V_2 is pulled down to $V_{DD} + V_{clk}$. V_3 is pulled up to $V_{DD} + 3 * V_{clk}$. V_2 is pulled down to $V_{DD} + 3 * V_{clk}$. V_{out} remains at $V_{DD} + 4 * V_{clk}$.

From Figure 2.5, when the threshold voltage of diode is ignored, the first stage will stabilize at V_{DD} and $V_{DD} + V_{clk}$. The second stage will stabilize at $V_{DD} + V_{clk}$ and $V_{DD} + 2 * V_{clk}$. The third stage will stabilize at $V_{DD} + 2 * V_{clk}$ and $V_{DD} + 3 * V_{clk}$. The forth stage will stabilize at $V_{DD} + 3 * V_{clk}$ and $V_{DD} + 4 * V_{clk}$. It can be concluded that the output voltage in stead state is related to the number of stages, the value of voltage supply and the clock voltage. Extend to N stages, the output voltage can be expressed as:

$$V_{out} = V_{DD} + N * V_{clk} \tag{2.29}$$

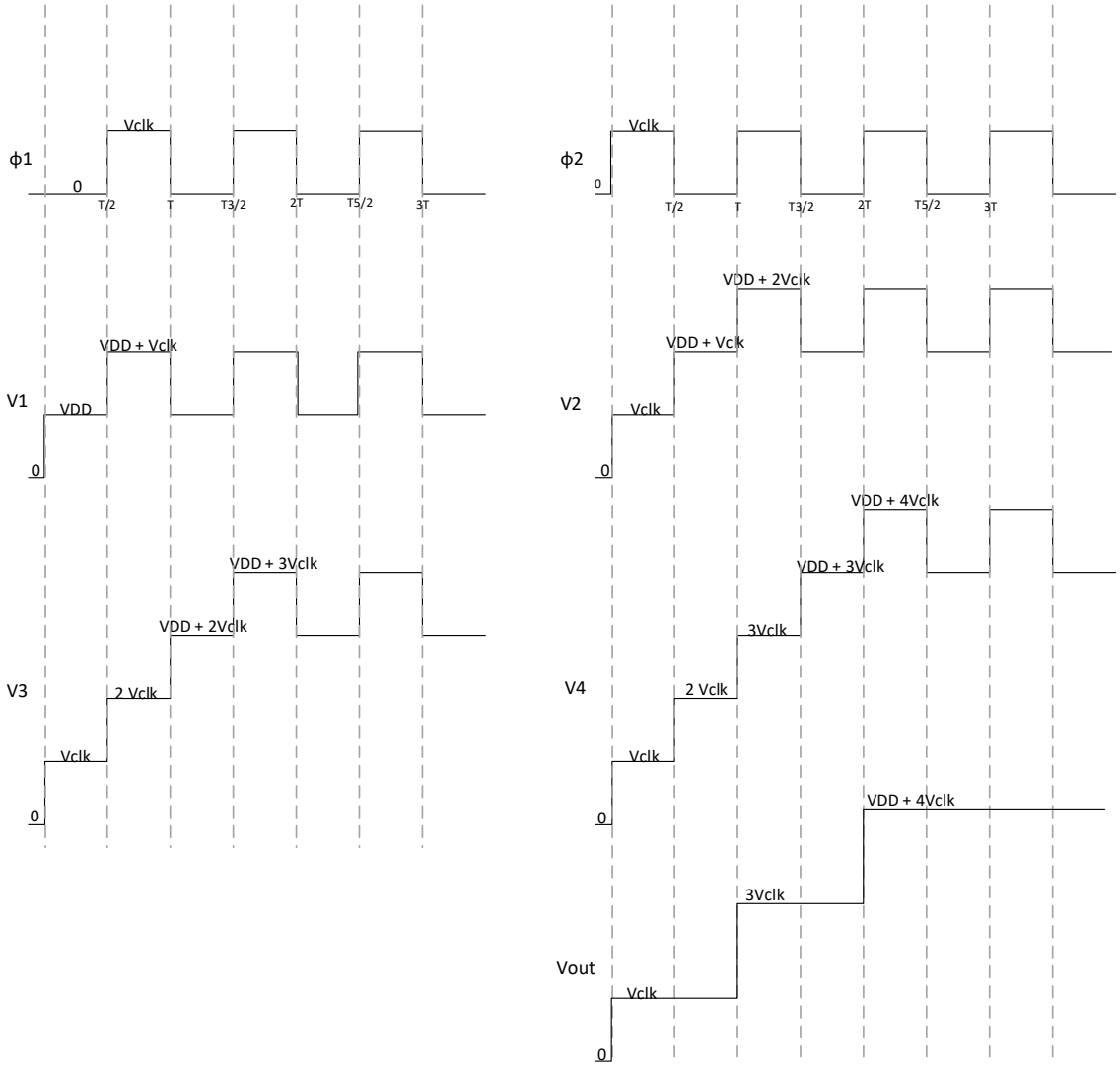


Figure 2.5: Dynamic process of V_1 to V_4 and V_{out} ignoring Vth

In practical applications, we usually use a MOSFET, whose gate and drain are connected to act as a diode. During the operation of the charge pump, the threshold voltage V_{th} of the MOSFET cannot be ignored. The performance of charging in each stage suffers at least a threshold voltage drop in MOSFET. So for the first stage, the stable voltage will be $V_{DD} - V_{th}$ and $V_{DD} + V_{clk} - V_{th}$. The stable voltage of the second stage will be $V_{DD} + V_{clk} - V_{th}$ and $V_{DD} + 2 * V_{clk} - 2 * V_{th}$. The third stage will stabilize at $V_{DD} + 2 * V_{clk} - 2 * V_{th}$ and $V_{DD} + 3 * V_{clk} - 3 * V_{th}$. The forth stage will stabilize at $V_{DD} + 3 * V_{clk} - 3 * V_{th}$ and $V_{DD} + 4 * V_{clk} - 4 * V_{th}$. And the difference between the 4^{th} stage and the output voltage is also a threshold voltage drop, so the output stage is $V_{DD} + 4 * V_{clk} - 4 * V_{th} - V_{th} = V_{DD} + 4 * V_{clk} - 5 * V_{th}$. The waveform of voltage V_1 to V_4 and V_{out} is shown in Figure 2.6.

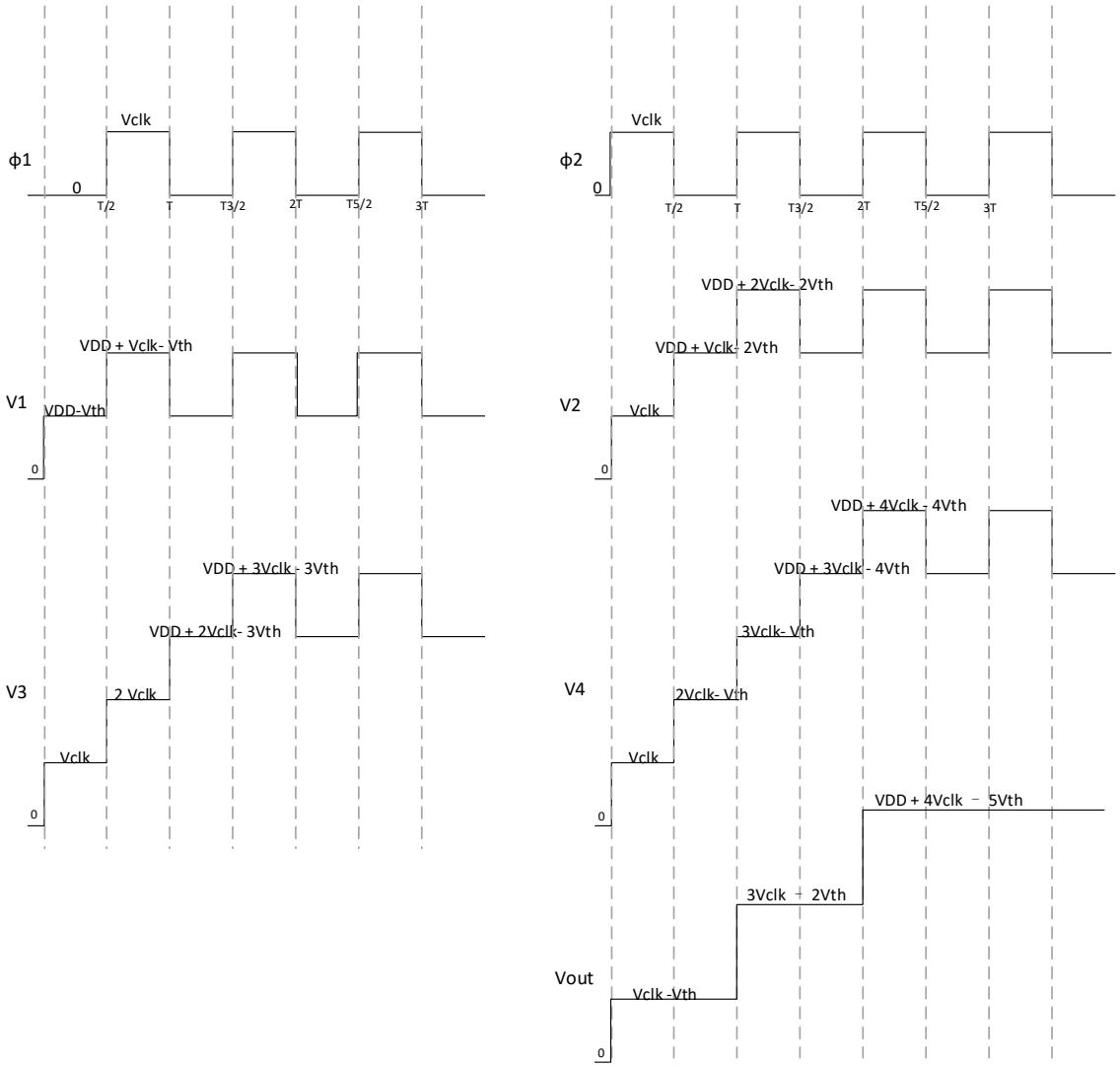


Figure 2.6: Dynamic process of V_1 to V_4 and V_{out} considering Vth

Extend to N stages, the output voltage can be expressed as:

$$V_{out} = V_{DD} + N * (V_{clk} - V_{th}) - V_{th} \tag{2.30}$$

It's worth mentioning that Equation 2.30 is obtained by assuming each MOSFET has constant values of threshold voltage.

The situation discussed above is where no load is added. It is more realistic to discuss the case of adding load. The schematic of charge pump with load is similar to the schematic of charge pump without load. The only difference is that a current source is added at the output to draw current from the circuit and to act as a load, shown in Figure 2.7.

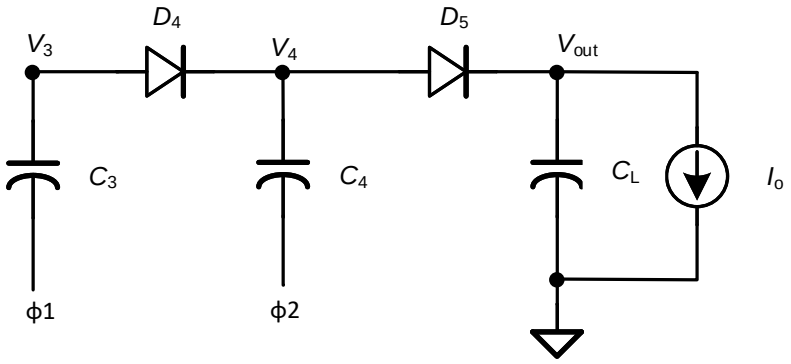


Figure 2.7: Part of the schematic of a 4-stage charge pump with loading current

Since the topological structure of the intermediate stage in the process of charging and discharging has not changed, the dynamic analysis process after adding a load is the same as when no load is added. Only the voltage pumped to the next stage ΔV at the rising edge of the clock changed. When there is no load for the charge pump circuit, ΔV is ideally considered to be V_{clk}. However, in practical, ΔV is influenced by V_{clk}, capacitance in each stage, parasitic capacitance, clock frequency as well as the loading current, which can be expressed as[19]:

$$\Delta V = V_{clk} \cdot \frac{C_i}{C_i + C_p} - \frac{I_o}{f \cdot (C_i + C_p)} \tag{2.31}$$

where V_{clk} is the high voltage of the clock pulse, C_i is the capacitor in each stage, C_p is parasitic capacitance, I_o is the loading current and f is the frequency of clock pulse. In this dissertation, the parasitic capacitance is temporarily ignored, so the expression of ΔV can be written as

$$\Delta V = V_{clk} - \frac{I_o}{f \cdot C_i} \tag{2.32}$$

Analyze the charging and discharging process as in the previous section, the expression of N^{th} stage and output voltage can be derived as

$$V_N = V_{DD} - N * (\Delta V - V_{th}) \tag{2.33}$$

$$V_{out} = V_{DD} - N * (\Delta V - V_{th}) - V_{th} \tag{2.34}$$

Since ΔV is smaller than V_{clk}, the voltage can be pumped each stage is lower. To get the same output voltage, more stages are needed.

2.2.2 Settling time

From Figure 2.6, we can not only draw the conclusion that the output voltage is related to the number of stages, but also can see from the figure that the time required for each stage voltage to reach a stable state is different. With i ($1 \leq$ i $\leq$ N) increasing, the time increased. And for the output stage, the time needed to get a stable voltage is called settling time. As analyzed in Equation 2.27, it takes time j for the output voltage to increase from $V_{DD} - V_{th}$ to $V_{out,j}$. When the needed output voltage is defined as V_{PP}, then settling time $T_{settling}$ is calculated:

$$V_{PP} = (N+1)(V_{DD} - V_{th}) - N(V_{DD} - V_{th})\beta^{T_{settling}} \tag{2.35}$$

$$T_{settling} = \frac{ln[\frac{(N+1)(V_{DD}-V_{th})-V_{PP}}{N(V_{DD}-V_{th})}]}{ln\beta} \tag{2.36}$$

with $\beta = 1/(1 + \frac{c}{NC_{out}})$, C_{out} is calculated in Equation 2.20 and Equation 2.21.

2.2.3 Ripple

As a switching power supply, charge pump circuits introduce system noise that can be fatal to state-of-the-art data converters, RF radios, phase-locked loops, etc[20]. To suppress noise,low dropout (LDO) regulator is normally cascaded to the switched supply. And providing low output ripple voltage from the charge pump is a feasible method to suppress the noise[20]. In addition, a big output ripple may impact the stability of RRAM write performance[21]. Hence, allowable voltage drop(ripple) is necessary in power supply design.

In Figure 2.6, the output voltage of Dickson charge pump keeps constant in stead state when no load current is added. However, after adding a load current, the output voltage is not a constant value, but changes with the rising and falling edges of the clock. Figure 2.8 shows the changes of output voltage and 4^{th} stage voltage V_4 in one period when charge pump has reached steady state.

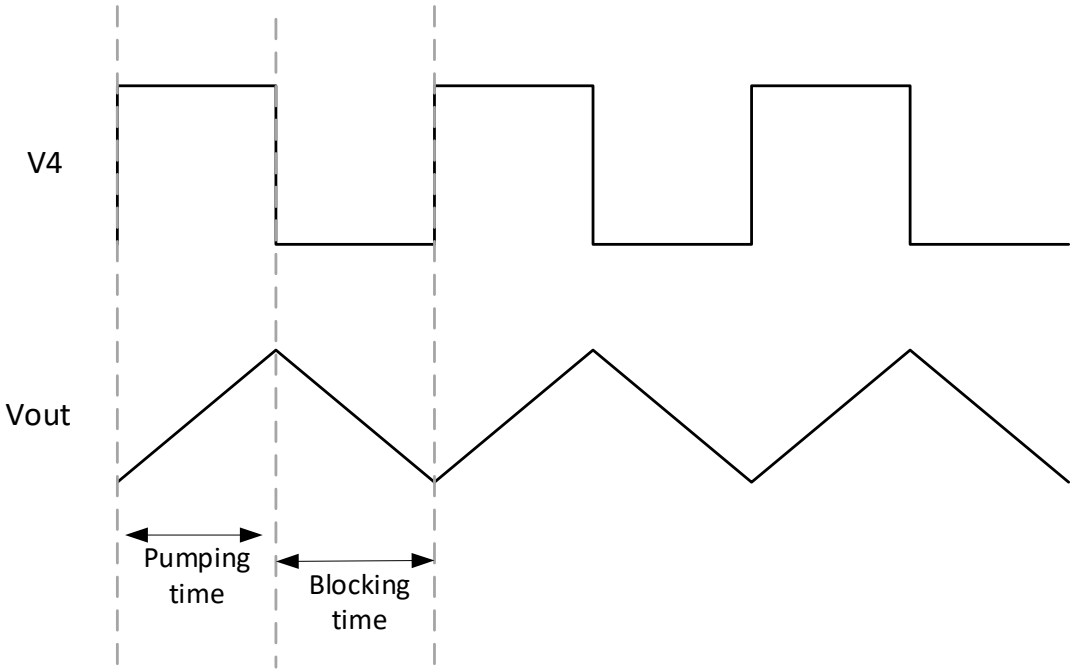


Figure 2.8: Figure of V_4 and ripple

In Figure 2.8, one period is divided into two part, half of the period is the blocking time and another half of the period is pumping time. When the clock of the last stage is low, the output voltage is at blocking time. The output capacitor is discharged by the loading current,so the output voltage will go down; When the clock of the last stage is high, the output voltage is at pumping time. The output capacitor is charged by the capacitor in last stage,then the output voltage will go up. The deviation of the voltage during the discharging process(also the charging process) is the ripple. As the amount of the transferred charge is equal, the ripple of the output voltage is given by

$$rippple = \frac{I_o \cdot \Delta t}{C_L} = \frac{I_o}{2 \cdot f \cdot C_L} \tag{2.37}$$

where I_o is the loading current, Δt is time of charging or discharging,which is half of the clock period here, and C_L is the load capacitor at output node. Although its average value of output voltage does not vary with load current, from Equation 2.37, we can know that deviation of output voltage is determined by the loading current, the frequency as well as the output capacitor. To reduce the ripple, lower loading current, larger clock frequency and larger output capacitance is required. To reduce ripple means to minimize the voltage deviation. During the blocking time, the voltage drop is incurred due to charge loss.

$$\Delta V = \frac{I_o}{C_L} \cdot t \tag{2.38}$$

So there are three ways to reduce the voltage drop. Decrease the loading current, increase the load capacitance and increase the clock frequency. The first two methods are to reduce the slope of the V-t curve, so that the charge will be lost less in the same time. The last method is to discharge less time. So the total lost charge $q = I_o \cdot t$ is lower.

For a given value of ripple, decreasing clock frequency means increasing the output capacitor if the loading current is fixed(1 uA). Once frequency is determined, output capacitor can be calculated by Equation 2.37; vice versa. Larger output capacitor leads to larger area, which will increase the cost. However, at the same time, larger output capacitor also means smaller frequency, leading to lower power consumption. At the opposite site, smaller output capacitor means larger frequency, leading to more power consumption and incomplete charge transfer. So the design of load capacitance, load current, and clock frequency are closely related to each other. How to choose the specific value should be traded off according to the system design requirements.

2.2.4 Power Consumption

In a charge pump, the power consumption mainly occurs during the switching cycles of the charge pump circuit. Specifically, power is consumed during the charging and discharging of the capacitors in the charge pump circuit. During the charging cycle, the capacitors are charged up to the desired voltage level by drawing current from the power source. During the discharging cycle, the capacitors discharge and provide current to the load. For a realistic charge pump circuit, power current consists of two parts. One part is the current consumption in a ideal charge pump at steady stage I_{ideal} and another part is due to parasitic effects $I_{parasitic}$.

$$I_{power} = I_{ideal} + I_{parasitic} \tag{2.39}$$

As the charge provided by the voltage source is transferred to the load stage by stage, I_{ideal} can be expressed as[22]:

$$I_{ideal} = (N+1)I_o \tag{2.40}$$

And the parasitic capacitors cause the nonideal part. In the process of charging and discharging, the parasitic capacitance of the upper and bottom plates of the capacitors of each stage C(i) require current. But because the parasitic capacitance value of the bottom board is much larger than other capacitance values. Therefore, approximately the bottom plate capacitance can be considered as the parasitic capacitance C_p. As the bottom plate capacitance is proportional to the value of C(i), the parasitic current can be expressed as[23]:

$$I_{parasitic} = NC_pfV_{clk} = \alpha NCfV_{clk} \tag{2.41}$$

where α is the ratio of parasitic capacitance of a stage capacitance to stage capacitance, N is number of stages, C is the stage capacitance, f is the clock frequency and V_{clk} is the clock voltage. So the power consumption can be expressed as:

$$P = I_{power} * V_{clk} = [(N+1)I_o + \alpha NCfV_{clk}] * V_{clk} \tag{2.42}$$

Conclusion comes out that power consumption of the charge pump circuit is related to the number of stages, the total capacitance, the loading current, the frequency as well as the clock voltage. Combine Equation 2.34, Equation 2.39 and Equation 2.41, substituting the capacitance value with other parameters, the final expression can be derived as:

$$I_{power} = (N+1)I_o + \alpha\frac{N^2}{NV_{clk} + V_{DD} - V_{out}}V_{out}I_o \tag{2.43}$$

2.3 Break down voltage consideration

2.3.1 Break down voltage

There are several techniques available to ensure the normal operation of CMOS devices under high voltage conditions. While advanced nanoscale CMOS technology offers significant advantages in terms of area and power compared to other technologies like multichip solutions, or exotic technologies(e.g., silicon on insulator (SOI) and Bipolar-CMOS-DMOS) [24], it poses a challenge in terms of reduced voltage tolerance. The cross-sectional view of a standard triple-well CMOS process are shown in the Figure 2.9.

During the design process, it is necessary to satisfy two constraints:

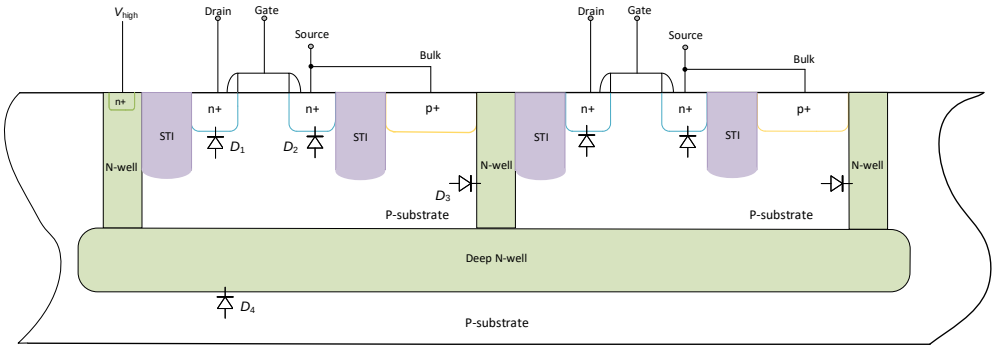


Figure 2.9: Cross-section of NMOS transistor layout in deep N-well

- Preventing forward biasing of the diode.
- Preventing the reversed bias voltage across the diode from exceeding the breakdown voltage.

The tolerance voltage of CMOS is the breakdown voltage of substrate diodes. Then the diode that needs to withstand the highest voltage needs to be found, which determines the breakdown voltage of the process.

In Figure 2.9, the bulk and source terminals are shorted to prevent back-gate bias effects. And each cell is isolated by N-well. 'Deep Nwell' is a method of isolation that can be employed for NMOS transistors in a PSUB (P-substrate) process. This method involves creating a deep nwell at the bottom and surrounding it with an nwell to form a ring, thereby isolating the transistor from noise interference caused by the common substrate and also improving device speed. If each cell is not separated by N-well, it means that all the bulk connections are joined together, and the buck is connected to the source of the last NMOS. As a result, the p-substrate becomes a high voltage, causing forward biasing of D_2, preventing the output voltage from reaching the expected value. So N-well is applied to separate each cell.

As can be seen in Figure 2.9, source terminal is connected to the drain terminal of the transistor in next stage, so V_{source} is the node voltage V_i in Figure 2.1. As bulk and source are shorted, the voltage drop between source and p-substrate is zero. Breakdown voltage of D_2 can be excluded from the scope of consideration. Then the breakdown voltage is determined by the tolerance voltage between drain and p-well V_{DP} (D_1) or the tolerance voltage between deep n-well and p-substrate V_{DNW} (D_4), or the tolerance voltage between n-well and p-substrate V_{NW} (D_3). It depends on the minimum of V_{DP}, V_{DNW} and V_{NW}.

Conventionally, N-well is connected to the highest voltage in the system, which is 20V here. When the source voltage of each stage is not high enough, the voltage on D_3 may exceed breakdown voltage, leading to breakdown of the transistor. And when N-well is connected to 20V, the voltage on D_4 may also exceed breakdown voltage . In order to solve the problem of breakdown voltage, a method called double-Diode substrate isolation is proposed in [24], which will be discussed in the next section.

2.3.2 DNW connection

Well breakdown voltage for 28nm CMOS is 10V[25], which is smaller than required output voltage 20V, depicted in Figure 2.10. An effective method to enhance voltage tolerance in [26] is by implementing an implant block mask to establish a lightly doped p-type buffer region encircling the n-wells. The buffer region, characterized by a lower doping concentration, leads to elevated junction breakdown voltages. However, only a few volts can be increased in this way. In [24], double-diode substrate isolation is proposed to increase more voltages.

The structure is illustrated in Figure 2.11. An intermediate voltage V_{mid} is introduced. As well breakdown voltage for 28nm CMOS is 10V, V_{mid} is designed as 10V here. Assuming that the output voltage of the k^{th} stage reaches 10V, for i less than k, the N-well of the i^{th} stage is connected to V_{mid}; for i larger than k, the N-well of the i^{th} stage is connected to V_{out} (20V). Then the maximum voltage over n-well/p-substrate diode(D_3 and D_7) is 10V. So D_3 and D_7 will not cause breakdown of transistors.

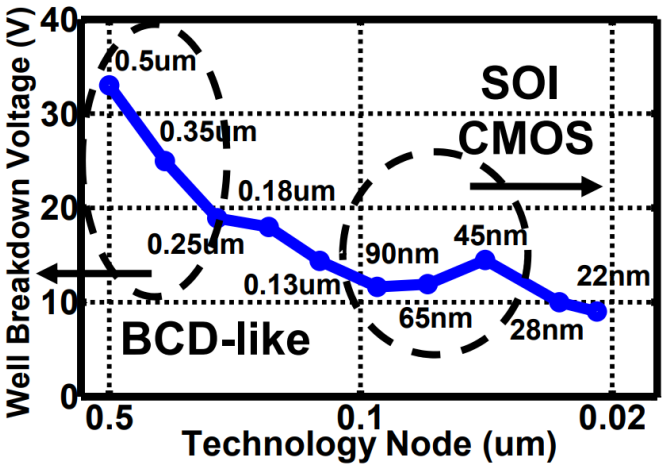


Figure 2.10: Breakdown voltage limitation[25]

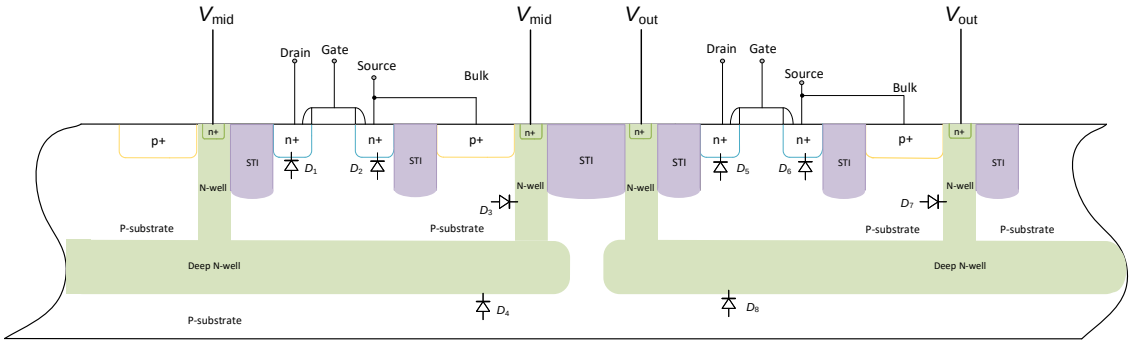


Figure 2.11: DNW connection

For the entire transistor, the maximum voltage it can withstand is the breakdown voltage of deep n-well/p-substrate diode, plus the breakdown voltage of source terminal/V_{mid} diode(D_2). So the available pumping voltage extends to 20V in 28-nm node.

But for this method, an issue still remains. Voltage over deep N-well/p-substrate diode(D_8) in i^{th} stage for i greater than k is still larger than the breakdown voltage for 28nm CMOS(10V).

3

Design of Dickson Charge Pump

According to the main factors considered in the charge pump design process introduced in Chapter 2, the actual design needs to comprehensively consider the output voltage, number of stages, ripple, power consumption, and area occupation. This chapter mainly discusses how to design various parameters of the Dickson charge pump circuit, including the size of diode-connected CMOS, capacitance value, frequency, how to optimize power consumption and the issues of Dickson charge pump.

3.1 Switch design

CMOS (Complementary Metal-Oxide-Semiconductor) transistors are commonly used as switches in charge pump circuits because they offer several advantages over diodes.

- Higher efficiency: CMOS switches have lower on-resistance and can handle higher currents than diodes, which results in higher efficiency and lower power dissipation.
- Lower voltage drop: The voltage drop across a diode can be significant, which reduces the output voltage of the charge pump circuit. CMOS switches have a much lower voltage drop, resulting in a higher output voltage.
- Better control: CMOS switches can be turned on and off more precisely and quickly than diodes, which allows for better control of the charging and discharging of the capacitors in the charge pump circuit.
- Smaller size: CMOS switches can be fabricated on a smaller scale than diodes, which can reduce the size and cost of the charge pump circuit.

The size of a transistor is critical to its performance and characteristics. The size of a transistor determines its maximum voltage and current carrying capacity, as well as its switching speed, driving capability, amplification ability, and power consumption. In modern integrated circuits, the smaller the size of a transistor, the lower its power consumption, the faster its speed, and the higher its integration density. Therefore, as integrated circuit manufacturing technology continues to develop, transistor sizes have been shrinking. However, with the continuous shrinking of transistor sizes, there are also challenges such as thermal effects and leakage current that need to be addressed through advanced process technology and transistor structure optimization. Therefore, the selection and optimization of transistor size are of great significance for the design and manufacturing of modern integrated circuits.

3.1.1 Length

When designing the transistor, not only the 'aspect ratio' W/L needs to be considered, but also $W \cdot L$, which is related to the area. During the design process, it is usually desirable to have a transistor with the smallest possible size to increase integration density and reduce power consumption. Therefore, selecting a small channel length of several micrometers at the beginning of the design process is a reasonable decision. Take the second stage for example, Figure 3.1 illustrates the structure of one stage when channel length is 4 um. As the maximum length of single NMOS is 2 um in 28-nm node, if a channel length that is greater than 4 um is needed, transistors can be designed to be connected in series. For example, when the channel length is designed as 4 um, two transistors are connected in series.

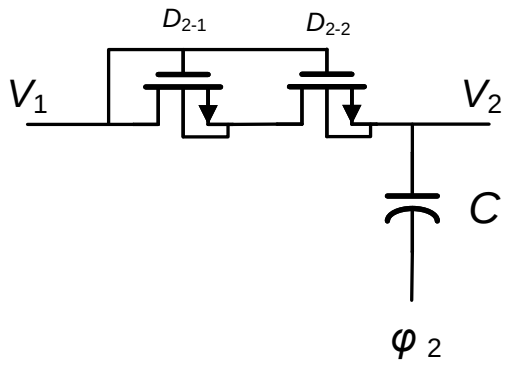


Figure 3.1: Structure of the second stage in Dickson charge pump

Build a 4-stage Dickson charge pump in Cadence, and keep the 'aspect ratio' W/L is 1/4. The simulation results of V_1 to V_3 with a channel length of 4 um without loading is shown in the Figure 3.2.

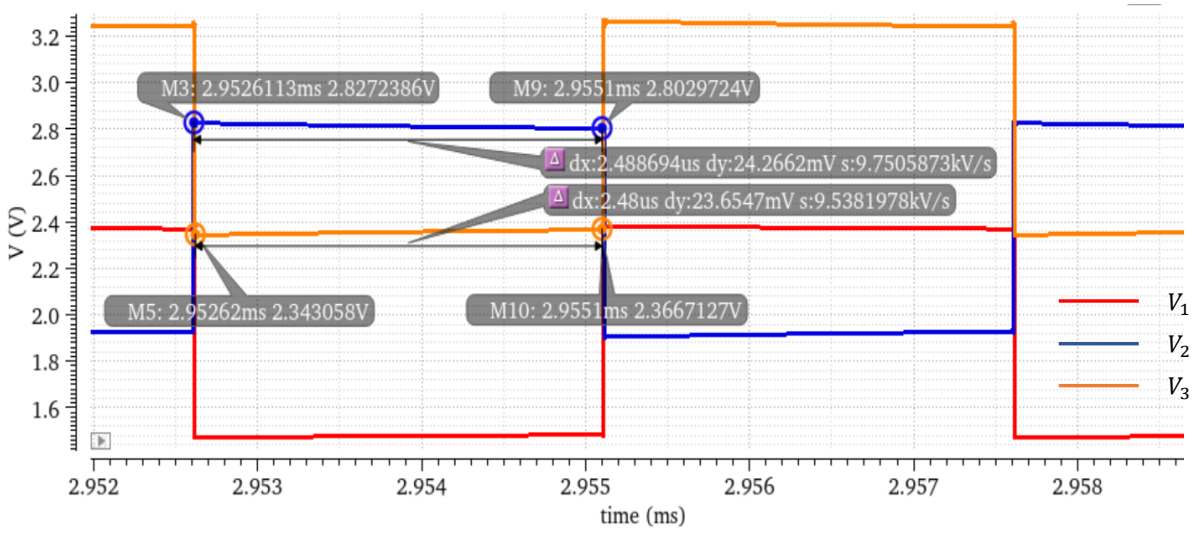


Figure 3.2: Channel length is 4 um with a width of 1 um

Figure 3.2 indicates one cycle of V_1 to V_3 in steady state, which shows that even in steady state, there is still a voltage drop of 24.27 mV across V_2 when clock is high. Two factors are considered as the reasons for voltage drop. One reason is charge sharing from V_2 to V_3 as V_2 is higher than V_3 . Another reason is the leakage current. When ϕ_2 is high, the transistor at the second stage D_2 should be turned off, and transistor at the third stage D_3 should be turned on. So V_2 will charge V_3 and V_2 will decrease. At the same time, there will be leakage current flowing through D_2. Although V_{GS} of D_2 (V_1 - V_2) is smaller than zero, V_{DS} of D_2 (V_2 - V_1) is larger than zero, which will cause charge flows from V_2 to V_1, leading to a voltage drop of V_2. Short-channel effect becomes more significant as the channel length decreases, which leads to an increase in leakage current[27]. So increasing the channel length can suppress leakage current. As can be seen in Figure 3.3, voltage drop of V_2 indeed decreases with a longer channel length of 6 um.

The generation of leakage current is due to the inability of the transistor to completely turn off in subthreshold region, leaving a current path. As the channel length of a CMOS decreases, the depletion region can extend over a significant portion of the channel, resulting in a reduction of the electron barrier height in the source region. In such a scenario, electrons at source and drain can diffuse into channel even

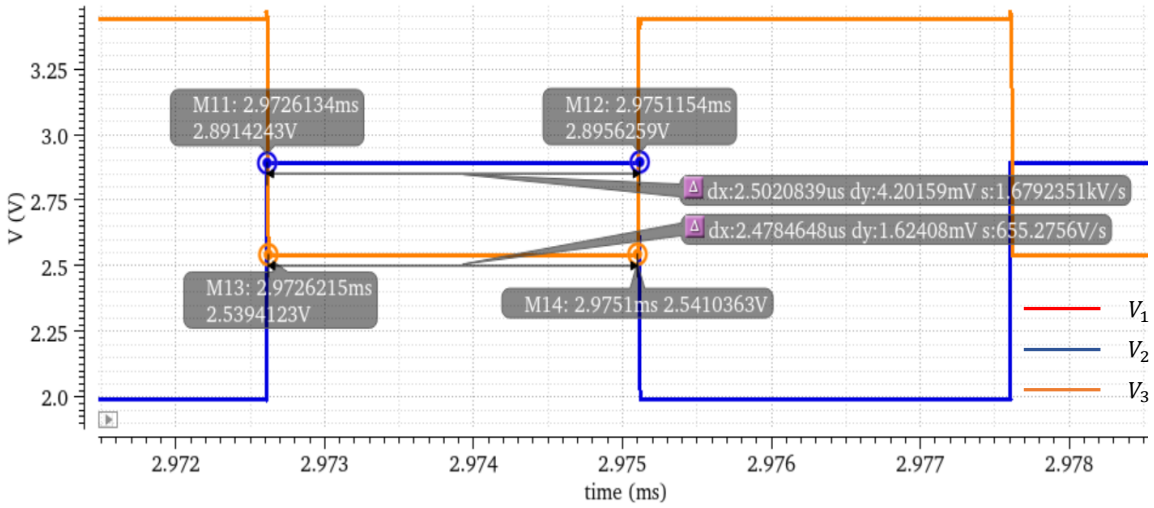


Figure 3.3: Channel length is 6 um with a width of 1.5 um

when the gate voltage is biased at 0V. If there is a voltage difference between source and drain, there will be a current, thus preventing the CMOS from being fully turned 'off'. Even when the transistor is in the off state, electrons can still flow through the oxide layer and into the channel region via the tunneling effect due to the presence of the depleted layer and oxide layer in the MOSFET.

The leakage current problem can be solved by increasing the channel length. Increasing the channel length can reduce the probability of tunneling and decreasing the leakage current. Additionally, increasing the channel length can improve the MOSFET's ability to withstand voltage. When the channel length of the MOSFET is short, the width of the depleted layer in the channel region is also short, resulting in a high electric field in the channel region. This increases the electric field that electrons need to overcome during the tunneling process and increases the probability of tunneling.

However, when the channel length is increased, the width of the depleted layer in the channel region also increases, reducing the electric field in the channel region and further decreasing the leakage current[28]. Increase the length reduces the electrical field strength, thus reduce the velocity of the electrons, resulting a smaller current density. So for small leakage, a longer channel length is desired. But the channel length cannot be too large, because large channel length leads to large parasitic capacitance, which will slow down the responding time, lower the efficiency and also needs a large area.

So there is an optimiazed value of channel length for the transistors in charge pump. The simulation data of the V_{out} VS channel length is shown in Figure 3.4. When increasing the channel length, the 'aspect ratio' keeps constant. From the Figure 3.4, it can be seen that when the channel length is greater than 6 um, the fluctuation of the output voltage is less than 50 mV, indicating that the increase in channel length at this point cannot significantly enhance the suppression of leakage current, or that the leakage current no longer dominates the voltage variation. Therefore, channel lengths within the range of 6 um to 12 um are all selectable. And the designed value is 6 um.

3.1.2 Width

When the circuit is unloaded, the current carrying capacity of the charge pump does not need to be considered. As the size of the transistor increases, the parasitic capacitance inside the transistor also increases, which can cause voltage drop in steady state if C_i is not large enough. And when size of transistors increase, the occupation of the total area also increases. As shown in Table 3.1, The output voltage does not increase significantly with the increase of the width. The width range from 500 nm to 10 um are all acceptable. For a small area, the minimum width of 500 nm is selected.

When the channel length is selected as 6 um and the width is 500 nm, the voltage waveforms of each stage in steady state are shown in the Figure 3.5 and Figure 3.6. The CMOS threshold voltage V_{th} can be calculated from the low voltage of V_1, which is 1.44V.

$$V_{th} = V_{th} - 1.44 = 0.36V \tag{3.1}$$

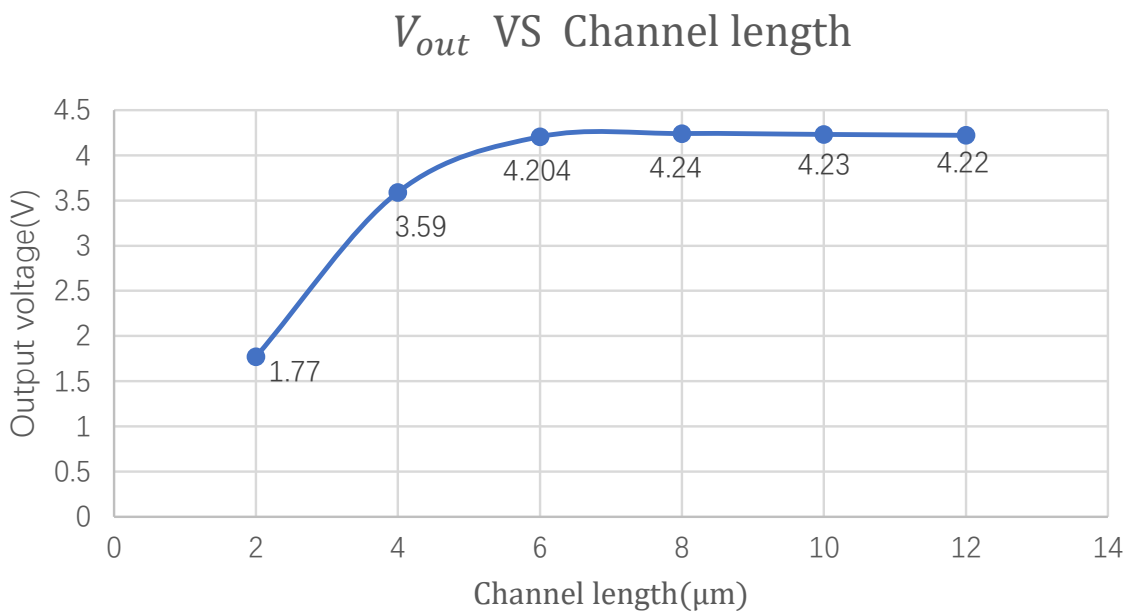


Figure 3.4: V_{out} VS channel length

$Width$	0.5u	1u	3u	5u	10u	20u	30u
V_{out}	4.22	4.23	4.24	4.24	4.23	4.19	4.16

Table 3.1: V_{out} VS different values of width

Substituting 0.36 V into the Equation 2.30, the stable voltage ranges from V_1 to V_4 are 1.44 V - 2.34 V, 1.98 V - 2.88 V, 2.52 V - 3.42 V, and 3.06 V - 3.96 V theoretically, which are exactly as the same as the simulation results.

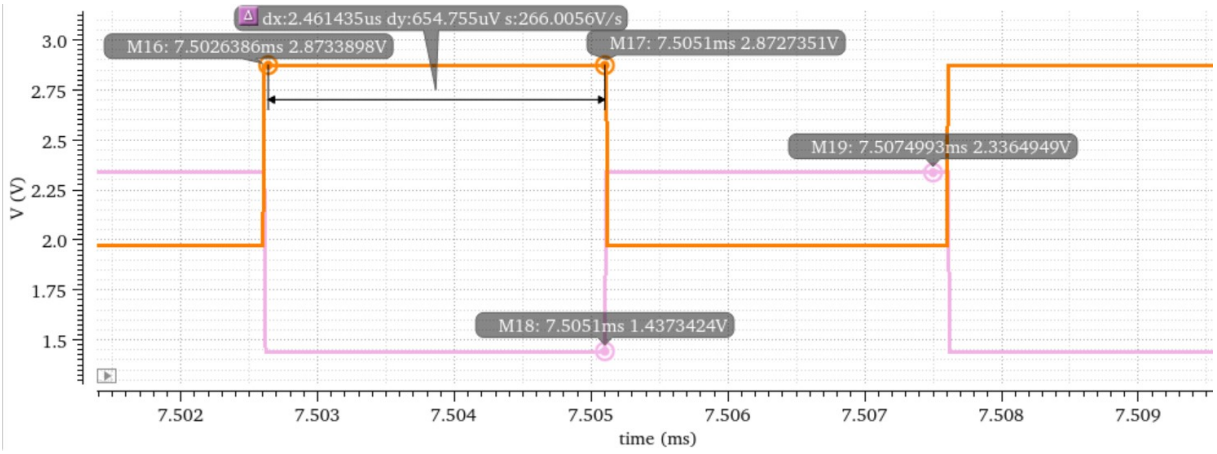


Figure 3.5: V_1(pink) and V_2(orange) in steady state without load

However, when loading current is added, the situation for the width of transistors is different. For example, when a load current of 1 uA is added, the simulation results in Figure 3.7 indicates that this circuit can not carry a load current of 1uA. At t=10 milliseconds, a current of 1 uA is introduced into the circuit. Prior to the introduction of the load current, the charge pump operates normally and the voltages keep rising. However, following the introduction of the load current, the voltages drop rapidly and stabilize at a low value within 1 millisecond. Even the first-stage voltage is not able to be charged to the expected value. Figure 3.8 is the simulation result of V_1 in steady state.

For the first stage, when the circuit reaches steady-state and the clock signal is low, V_1 should be stable

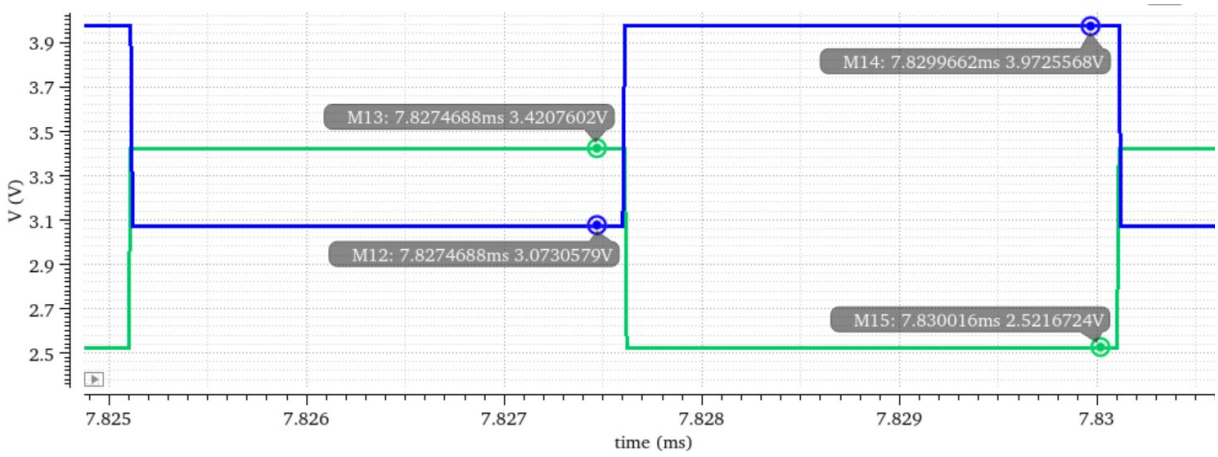


Figure 3.6: V_3(green) and V_4(blue) in steady state without load

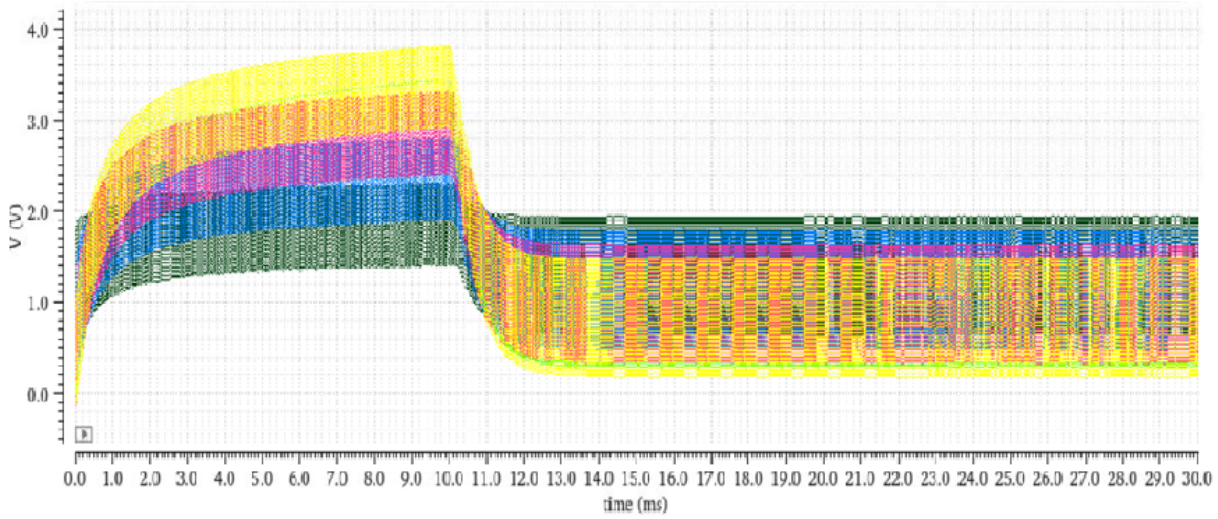


Figure 3.7: Voltages when 1 uA is added in small size MOSFET

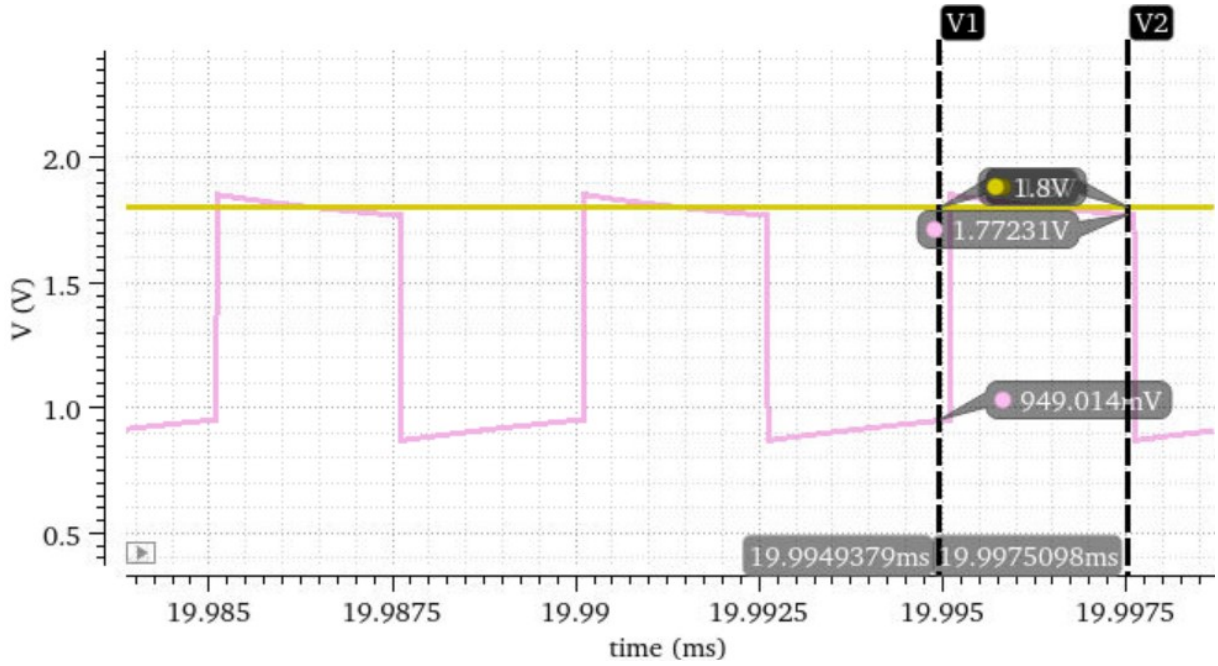


Figure 3.8: V_1 when 1 uA is added in small size MOSFET

at $V_{DD} - V_{GS}$. V_{GS} is the voltage between gate terminal and source terminal. From Figure 3.8, it can be seen that $V_{DD} - V_{GS}$ is lower than the expected value, indicating that V_{GS} is relatively high. This can also be understood from the individual cycle plot of the output voltage in Figure 2.8, where the output capacitor discharges during the low half-cycle of the first stage clock due to the load drawing charge, resulting in a decrease in voltage. To achieve a stable output, given that the load is always present, twice the loading current $2I_o$ is required to charge the output capacitor during the high half-cycle of charging. From the $I - V_{GS}$ curve in Figure 3.9, it can be inferred that the larger the current, the larger the V_{GS}. Therefore, $V_1 = V_{DD} - V_{GS}$ cannot be charged to a higher value.

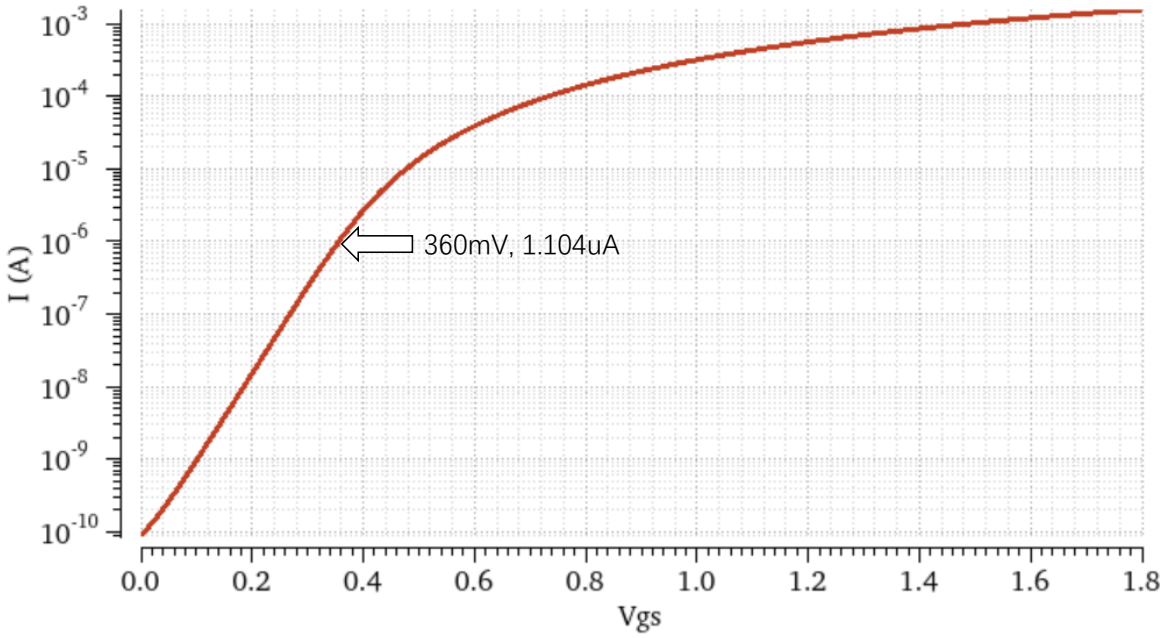


Figure 3.9: I_D VS V_{th}

In Figure 3.9, When loading current is 1 uA, the transistors work in strong inversion region, then the current I_D is proportional to the square of $V_{GS} - V_T$.The current expression can be written as[29]:

$$I_D = k' \frac{W}{L} \cdot (V_{GS} - V_T)^2 \tag{3.2}$$

where I_D is the drain current of the transistors, k' is a technological parameter linked to n, W and L are the width and length of the transistors respectively, V_{GS} is the the voltage between gate terminal and source terminal,and V_T is the threshold voltage. It can be inferred from Figure 3.9 that the larger the current, the larger the V_{GS}. Therefore, $V_1 = V_{DD} - V_{GS}$ cannot be charged to a higher value when loading current is large. From Equation 3.2, it can be deduced that to obtain a relatively small V_{GS} when the current is constant, the size of the transistor should be increased.

The leakage current can be calculated according to Equation 3.4:

$$I_{leakage} = \frac{C \cdot \Delta V}{t} \tag{3.3}$$

where C is the capacitance in each stage, ΔV is the voltage drop due to leakage current, and t is the time of voltage drop. Calculate the leakage current value without load according to the simulation results in Figure 3.5, and it is calculated as

$$I_{leakage} = \frac{C \cdot \Delta V}{t} = \frac{60 * 10^{-12} * 654.755 * 10^{-6}}{2.4614 * 10^{-6}} = 15.97nA \tag{3.4}$$

15 nA can be ignored compared to the loading current of 1 uA. So there is no need to increase the channel length.

Keep the length of CMOS constant, which is 6 um. Change width to change the 'aspect ratio' W/L. The following Figure 3.10 shows the results of V_{out} with different CMOS size W/L.

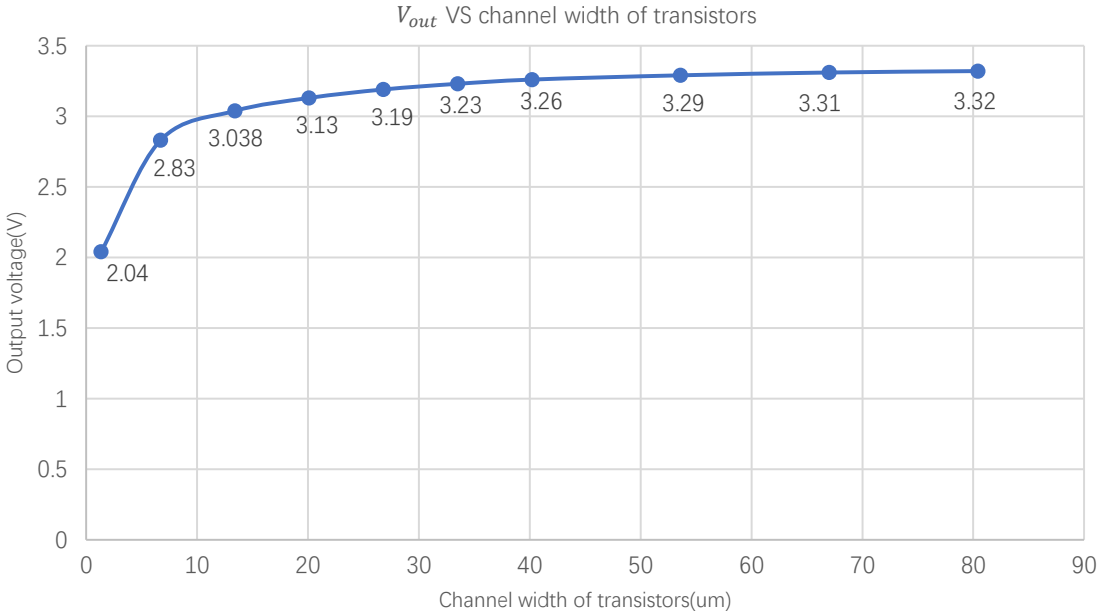


Figure 3.10: V_{out} VS channel width of transistors

For the same value of load current, after increasing the size of transistors, the output voltage goes up. Considering that increasing the transistor size too much would result in larger occupied area. And with further size increase, the voltage gain is not significantly improved, the W/L value of 40 um/ 6 um is chosen. Due to the maximum length of a single MOSFET being 2 um, three MOSFETs are connected in series to achieve a total channel length of 6 um. Each NMOS finger has a width of 1 um, with a total of 20 fingers and a multiplier of two, resulting in a total channel width of 40 um.

3.2 Area limit

In the design of a charge pump, the area occupied by the circuit is also an important consideration. A smaller area can lead to cost savings and greater integration density. However, this must be balanced with the performance requirements and limitations of the manufacturing process. The area occupation in charge pump is mainly due to transistors and capacitors.

The layout with the selected W/L of 40 um/ 6 um is shown in the Figure 3.11. The area occupation of NMOS in one stage is 1090.192 um^2.

The layout of buffer is illustrated in Figure 3.12. The occupied area of buffer in one stage is 37.71 um^2.

A capacitor layout is shown in the Figure 3.13. In the diagram, the CMOS finger width is 50 nm, finger length is 40 nm, finger spacing is 50 nm, and there are 200 fingers in total. The top metal layer is 6. The total capacitance value is 4.455 43 pF, and the area is 795.0539 um^2, resulting in a capacitance density calculation of 5.604 fF/um^2. For a capacitor with a capacitance of 60 pF, it occupies an area denoted as 10 706 um^2.

By comparing the sizes of capacitors, transistors, and buffers, it can be observed that the size of capacitors is much larger than the other two. So when calculating the circuit area, the transistor size can be ignored and only the capacitor area considered. The total circuit area formula can be approximated expressed as

$$Area = (NC_i + C_L) \cdot C_{density} \tag{3.5}$$

$C_{density}$ is the capacitance density. Equation 3.5 are mainly used when choosing the optimized value of capacitors.

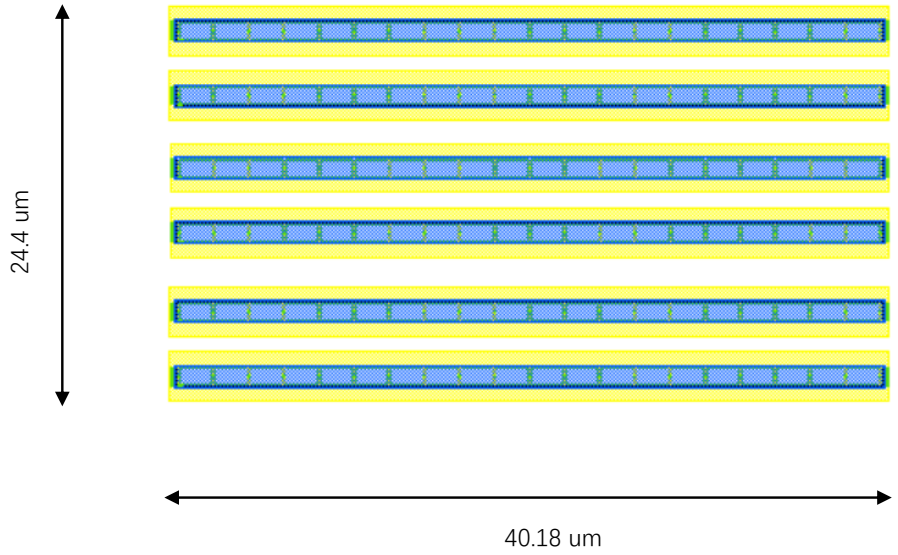


Figure 3.11: Layout of NMOS

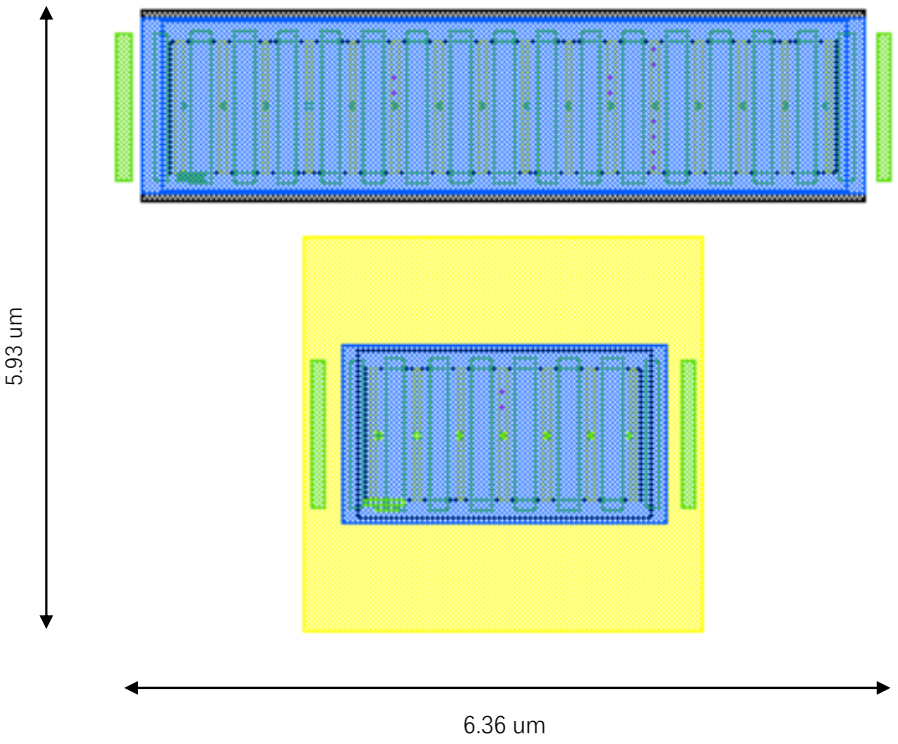


Figure 3.12: Layout of buffer

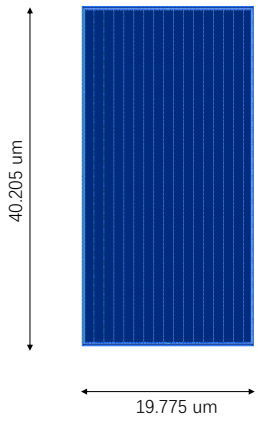


Figure 3.13: Layout of capacitor

3.3 Power consumption

When loading current is added, power consumption and efficiency must be taken into account. To calculate the power consumption, buffer is necessary for the circuit. The driving capability of a circuit mainly refers to two aspects. First, the output signal of the previous stage can be recognized by the next stage, which also means that the output voltage after adding the buffer should be able to reach the clock voltage value before adding the buffer. Second, the signal of the previous stage needs to be recognized by the next stage within a specified time, which means that the rise time of the buffer output voltage needs to be within a certain range. In order to provide a strong driving capability to the load and achieve optimal power dissipation along the time integral, buffer is added after the clock signal. The buffer is actually two series-connected inverters, which simulate the actual resistance of the MOSFET during conduction.

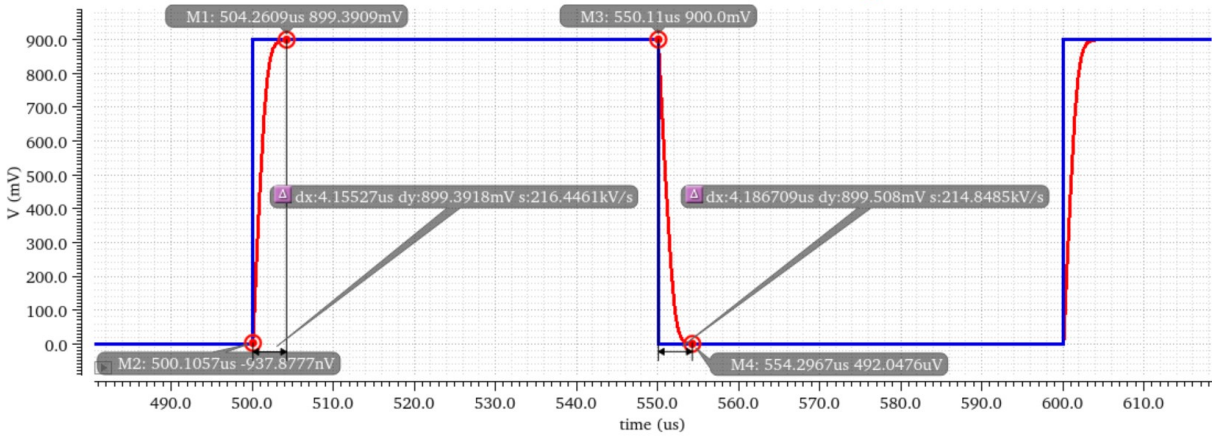


Figure 3.14: Test of buffer when load is 1 nF

When the PMOS width is 15um and length is 150nm, and the NMOS width is 6um and length is 150nm, the drive capability of the buffer for a 1pF load capacitor is shown in Figure 3.14. At this time, the clock signal voltage amplitude is 0.9 V. It can be clearly seen from Figure 3.14 that the load voltage can quickly reach 0.899V, which is 99.89% of the clock signal amplitude, and the load voltage can reach 0.899V within 4.2 us, with a response speed of 8.4% of the pulse width. Therefore, it can be concluded that the designed buffer still has a strong driving capability for a 1 pF load capacitor. Then two circuits were compared: one with a buffer and one without a buffer, whose results shown in Figure 3.15. For the output voltage of the four-stage charge pump, the maximum difference between the two scenarios is only

8 mV. It can be said that the buffer has no impact on the output voltage, so it can be used for power consumption analysis of the circuit.

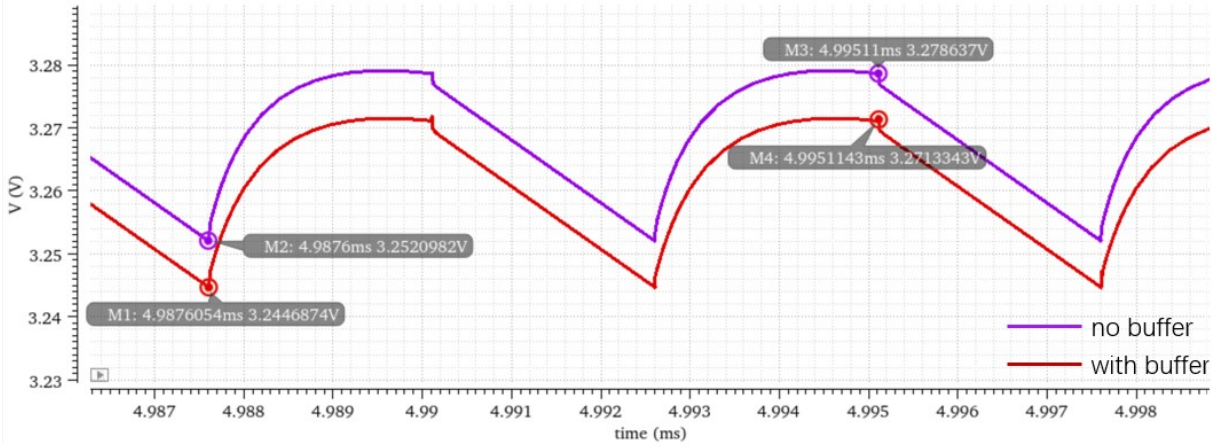


Figure 3.15: $Vout$ with buffer and without buffer

The total power loss in Dickson charge pump consists of three terms: the voltage drop in switch, output resistance of charge pump and the switching operations that involve the parasitic capacitances[30].

In addition to the load, MOSFET devices also consume power in the circuit. To quantitatively calculate the power consumption of MOSFET device, each stage can be equivalent to a resistor, and the power loss of each stage can be calculated, and then multiplied by the number of stages to calculate the power consumption of MOS devices in an N-stage charge pump. However, the equivalent resistance of each stage cannot be accurately calculated. Therefore, using the ratio of output power over input power is a better choice. When there is a load and buffer in the circuit, the output power can be expressed as the output voltage multiplied by the output current:

$$P_{out} = V_{out} \cdot I_o \tag{3.6}$$

Since both DC power supply and clock signal can power the circuit, the output power can be expressed as:

$$P_{in} = V_{DD} \cdot I_{in} + V_{clk} \cdot I_{buffer} \tag{3.7}$$

where I_{buffer} is the current flowing through buffer. So the expression of power efficiency is derived as:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_o}{V_{DD} \cdot I_{in} + V_{clk} \cdot I_{buffer}} \tag{3.8}$$

3.4 Capacitor size choice

3.4.1 Capacitor in each stage

According to the discussion in Chapter 2, to achieve a certain output voltage, the capacitance value in each stage C_i is related to the number of stages and the settling time. As analyzed in Section3.2, the circuit area is mainly related to the capacitance value in each stage, so increasing C_i to infinity is not a good choice.

When the value of C_i is small, more stages are required to achieve the desired output voltage of 20V. When the value of C_i is large, although fewer stages are needed to achieve the desired output voltage, each stage occupies a larger area. Therefore, considering only the chip area, there is an optimal value for the capacitor C_i. When a loading current of 1 uA and output voltage is 20 V, the relationship between capacitance and area/capacitance density is shown in Figure 3.16.

The horizontal axis represents different capacitance values, and the vertical axis represents area divided by capacitance density. The chart is based on simulation data for a four-stage charge pump and Equation 2.34 . For a given capacitance value, since the load current and frequency are constant, the pumping voltage

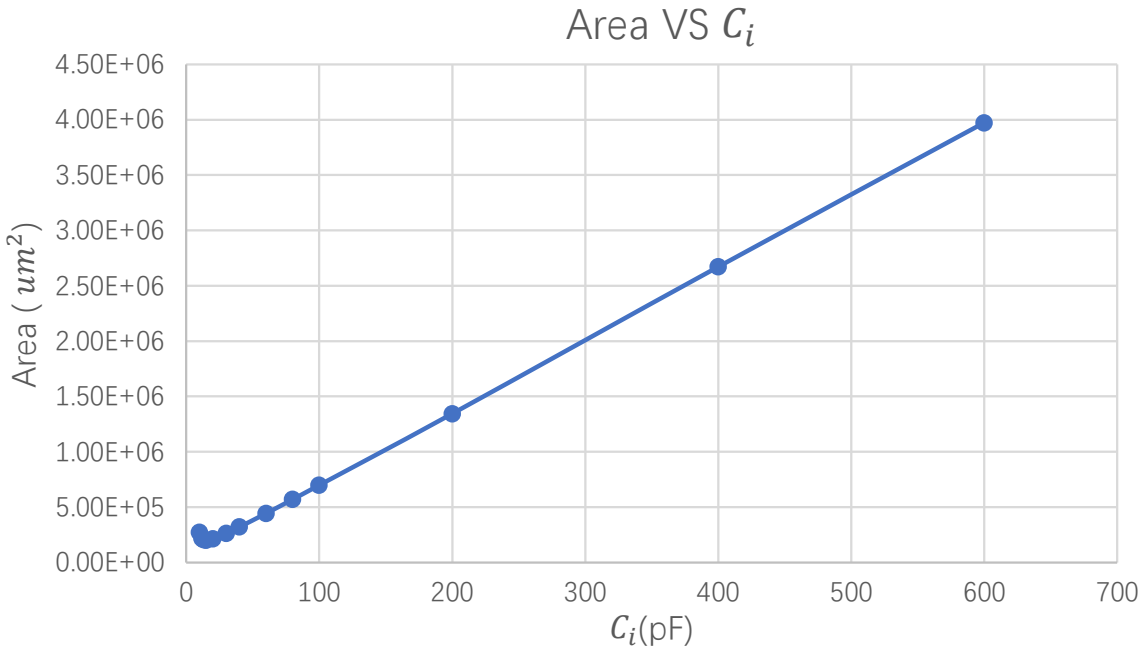


Figure 3.16: Area VS C_i

ΔV of each stage is equal, which can be calculated using Equation 2.32. Equation 2.34 can be used to derive the number of stages required to achieve an output voltage of 20 V, and then the area required for implementing a 20 V output can be calculated. For example, when the capacitance is 60 pF, the low voltage at steady state for the first stage is 2.25 V, the output voltage $V_{out,4}$ is 3.26 V, and the threshold voltage V_{th} is 0.36 V. The relationship between the output voltage and V_1 for the four-stage charge pump is:

$$V_{out,4} = V_1 - 3 * (\Delta V - V_{th}) - V_{th} \tag{3.9}$$

Assuming that n stages are needed to achieve an output voltage of 20 V, then

$$V_{out,n} = V_1 - (n-1) * (\Delta V - V_{th}) - V_{th} \tag{3.10}$$

Combining Equation 3.9 and Equation 3.10, the value of n can be calculated as 40.65. Since stage should be integer, n is chosen as 41. Figure 3.17 shows the output voltage when stage is 41. The pss simulation results shows that the rms value of output voltage is 20.18 V. The simulated stage is exacyly same as the calculated results.

Therefore, it can be concluded that the results of the four-stage charge pump can be used to calculate the area required for a 20 V output.

In Figure 3.16, when C_i is relatively small or large, the relationship between area and capacitance is different. Therefore, Figure 3.16 is divided into two parts for analysis, which are shown separately as Figure 3.18 and Figure 3.19. In Figure 3.18, when C_i is smaller than 15 pF, as the capacitance value decreases, the area does not decrease but instead increases. This is because, for small capacitance values, the number of stages required to achieve a 20 V output increases significantly. The increase in the number of stages dominates over the decrease in capacitance, resulting in an overall increase in area.

When the capacitance value is large, the increase in capacitance dominates over the number of stages in $n \cdot C$. After a certain point, according to Equation 2.32, the pumping voltage of each stage ΔV remains almost constant, so the number of stages almost does not change with increasing capacitance. Therefore, the relationship between area and capacitance can be approximated as linear, which is the situation in Figure 3.19. The trend of area in Figure 3.19 can be calculated.

According to Equation 3.10, the number of stages, n, can be expressed as

$$n = \frac{V_{out,n} - V_1 + V_{th}}{\Delta V'} + 1 = \frac{m}{\Delta V'} + 1 \tag{3.11}$$

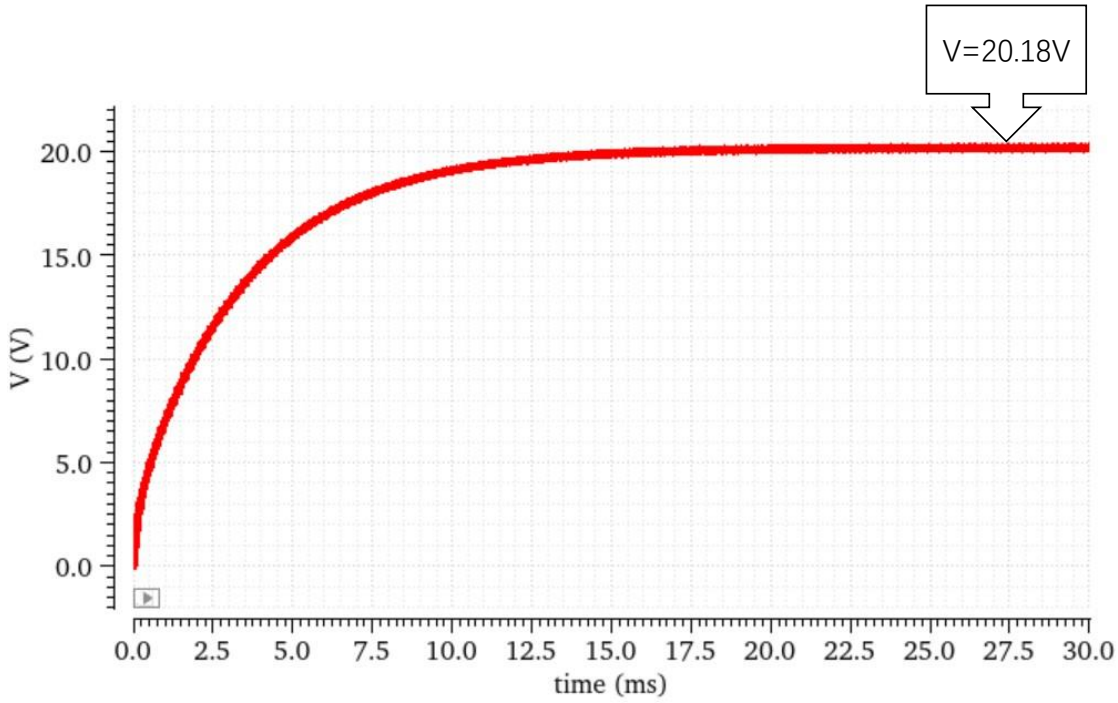


Figure 3.17: V_{out} of 41-stage charge pump

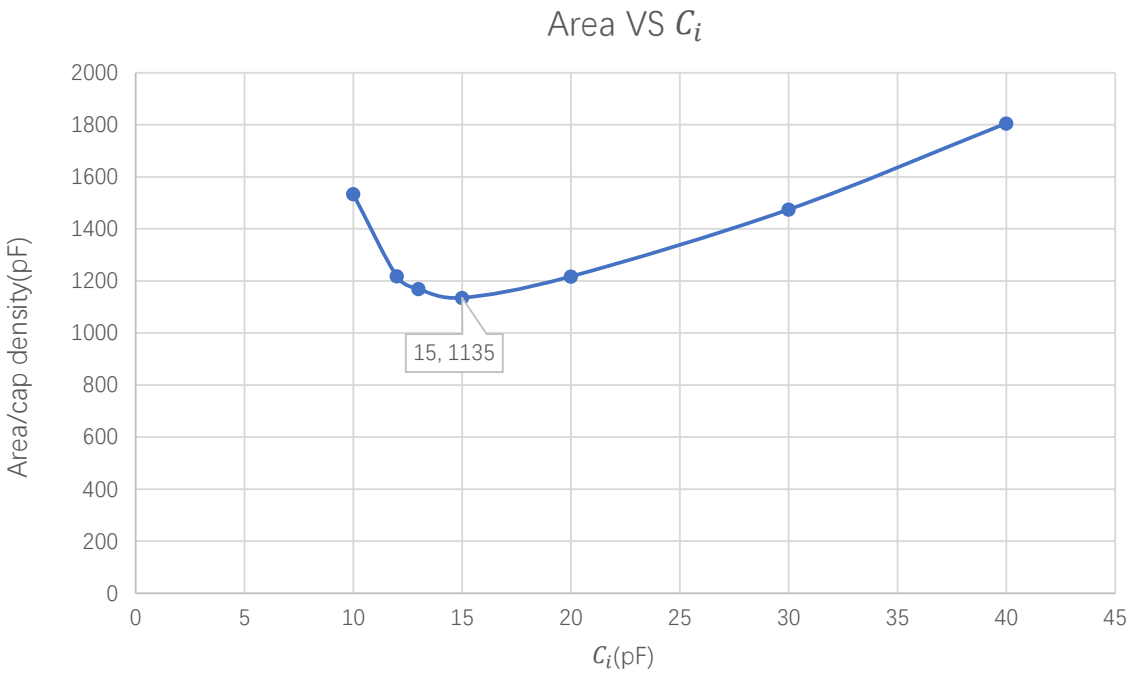


Figure 3.18: Area/cap density VS small C_i

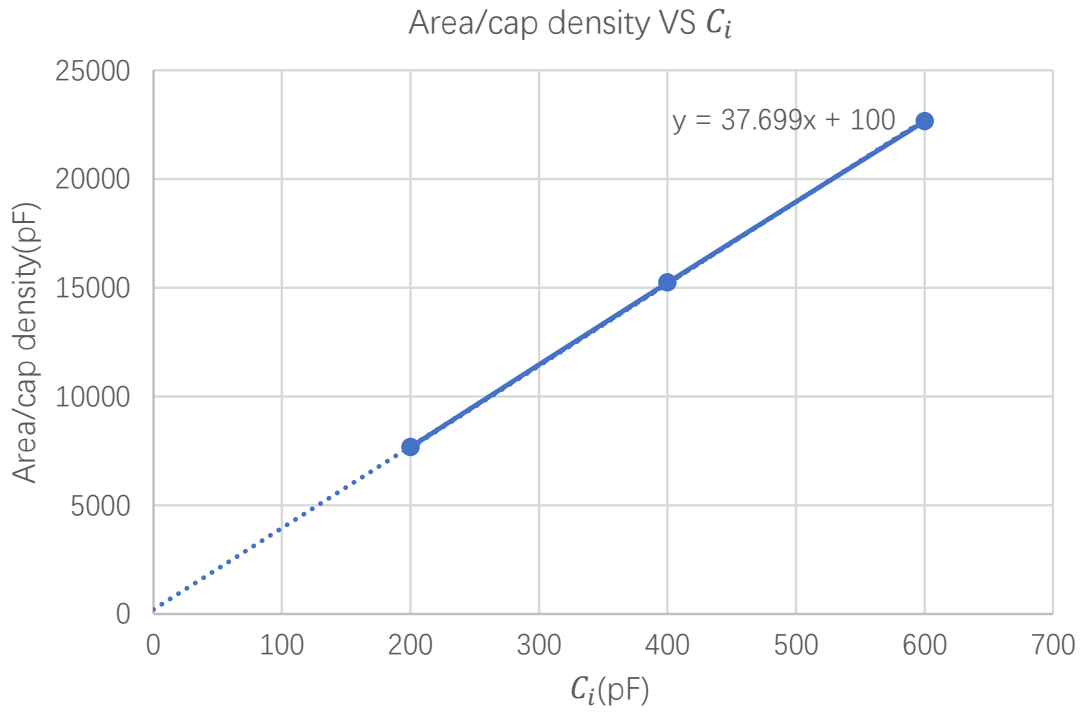


Figure 3.19: Area/cap density VS big C_i

where m is $V_{out,n} - V_1 + V_{th}$, and $\Delta V'$ is related to C_i, which can be approximated as

$$\Delta V' = V_{clk} - \frac{I_o}{f \cdot C_i} - V_{th} = \frac{\alpha}{C_i} + \beta \tag{3.12}$$

from which $\alpha = -\frac{I_o}{f}$ and $\beta = V_{clk} - V_{th}$. Substituting Equation 3.12 into Equation 3.5, the area can be derives as

$$Area \propto (\frac{m}{\frac{\alpha}{C_i} + \beta} + 1) \cdot C_i + C_L \propto (\frac{mC_i}{\alpha + \beta C_i} + 1)C_i + C_L \tag{3.13}$$

When C_i is large enough,

$$\frac{mC_i}{\alpha + \beta C_i} \approx \frac{m}{\beta} \tag{3.14}$$

Then area can be derived as:

$$Area \propto (\frac{m}{\beta} + 1)C_i + C_L \tag{3.15}$$

From Equation 3.15, it can be concluded that the slope of curve 'Area/capdensity VS C_i' is the number of stages n, and the offset is C_L.

If only consider the aspect of area, then the optimal value of capacitance is 15 pF.

But in practical, power consumption and efficiency are also considered as important considerations when design the value of C_i.

According to Figure 3.20, when C_i is small, as the capacitance C_i increases, the efficiency of power consumption also increases. However, when the capacitance reaches a certain value, the efficiency remains almost constant. But when C_i is smaller than 10 pF, voltage can not be pumped anymore, so the graph starts at $C_i = 10$ pF. When C_i is larger than 200 pF, power efficiency approximately stabilizes at 55%. From Equation 3.8, the power efficiency is related to the output voltage V_{out}, the loading current I_o, and the current flowing through buffer I_{buffer}. From Equation 2.34 and Equation 2.32, with C_i increasing, V_{out} also increases. The loading current is fixed. And since the constant frequency, the power consumed by buffer is only related to the total capacitance including parasitic capacitance.

The power of the buffer increases as the capacitance increases, but this incremental increase is very small and can be approximated as almost constant. Therefore, in the power expression, the increase in output power dominates as the capacitance increases, so the larger the capacitance, the higher the efficiency. However, when the capacitance is very large, the output voltage hardly changes with changes in capacitance. Therefore, when the capacitance is very large, the efficiency stabilizes at a certain value.

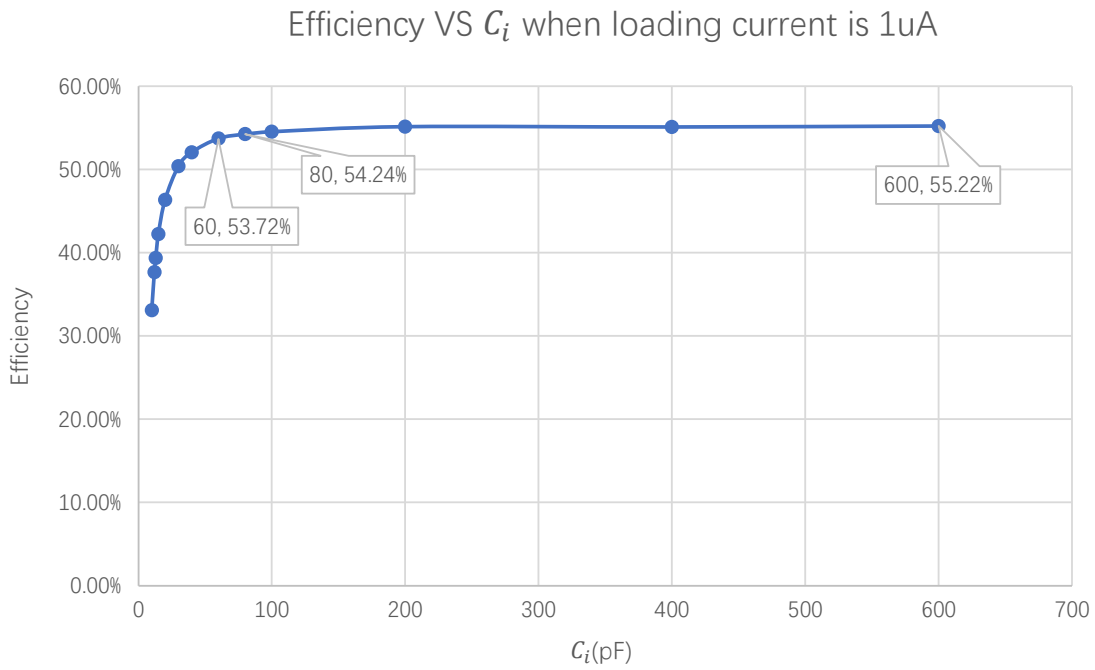


Figure 3.20: Efficiency VS C_i when I_o is 1 μ A

From Figure 3.20,it can be concluded that when the capacitance is 60 pF or 80 pF, the efficiency has almost reached its maximum value for the given load. Continuing to increase the capacitance will only increase the area without further increasing the efficiency. Therefore, when the load is 1 uA, considering both power efficiency and area, the optimal value for the capacitance is 60 pF or 80 pF. In further discussion, 60 pF is chosen.

3.4.2 Output capacitor

The output capacitor C_L influence the value of ripple as analyzed in Section 2.2.3. When frequency is fixed, C_L is inversely proportional to the ripple. When loading current is 1 uA and frequency is at 200 kHz, the relationship between capacitance and ripple should be expressed theoretically as:

$$rippple = \frac{I_o \cdot \Delta t}{C_L} = 2.5 \cdot 10^{-12} C_L^{-1} \tag{3.16}$$

Figure 3.21 shows the simulation results of ripple VS C_L, which matches well with the calculated results. In order to reduce the ripple of the output voltage, an output capacitor of 100 pF is selected. At this time, the ripple is 25 mV, which is 1.25% of the output voltage.

3.5 Frequency choice

The frequency of operation is essential in a charge pump because it affects the efficiency, output voltage ripple, and output current of the circuit. At a given load, to achieve the expected voltage, higher frequency is preferred[31]. But unrestrained increase in frequency will reduce power efficiency.

The relationship between efficiency and frequency is shown in the Figure 3.22.

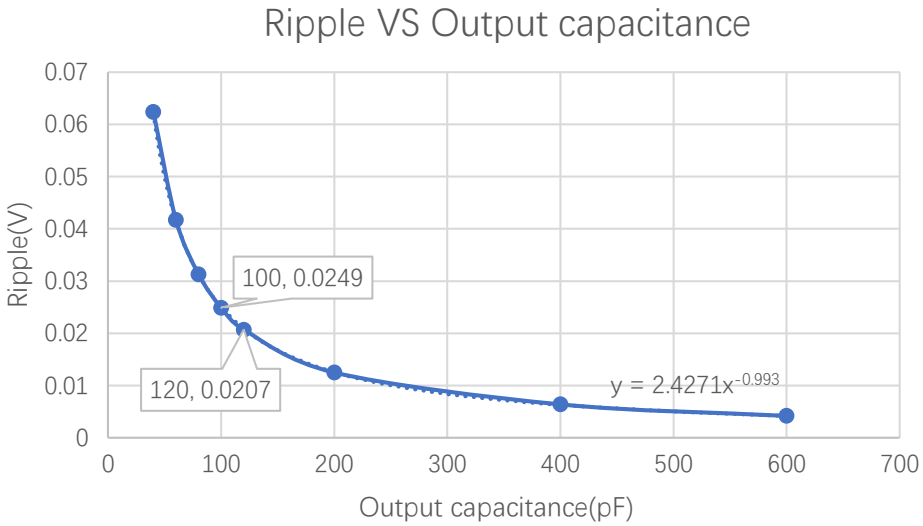


Figure 3.21: Ripple VS output capacitor

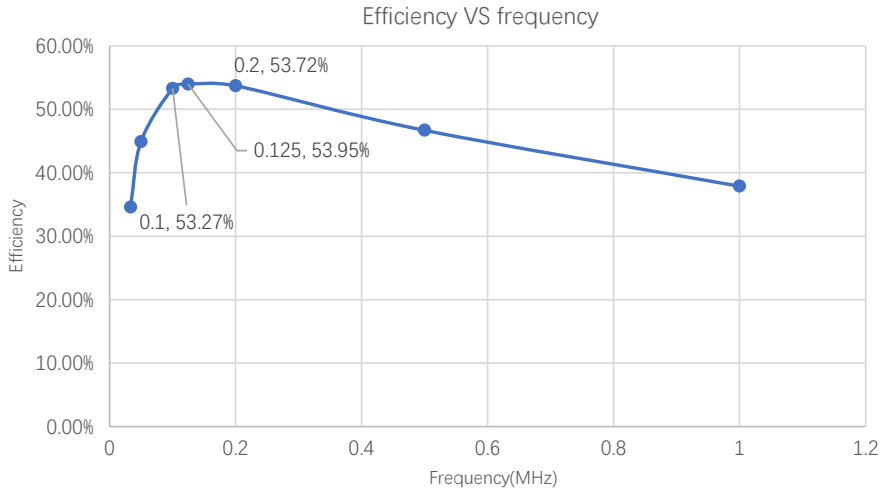


Figure 3.22: Efficiency VS frequency

The efficiency of the charge pump increases with increasing frequency because more charge is transferred per unit time. However, When the frequency increases to a certain value, increasing the frequency will not improve efficiency, but rather decrease it. This can be analyzed from the perspective of ΔV. When the frequency is very high, ΔV does not change significantly with frequency, which means that increasing the frequency will not significantly increase the output voltage, and therefore the output efficiency remains relatively constant. However, at the same time, the power consumed by the buffer increases as the frequency increases, leading to a decrease in circuit efficiency. For the efficiency, frequency at 125 kHz and 200 kHz can both considered as the optimal frequencies.

But frequency will also influence ripple. As analyzed in chapter 2, high frequency also leads to small ripple. When choosing the stage capacitance of 60 pF, and a output capacitance of 100 pF, the relationship between output ripple and switching frequency is shown in Figure 3.23, the higher frequency, the lower ripple when output capacitance is fixed. So 200 kHz is chosen as the optimal frequency.

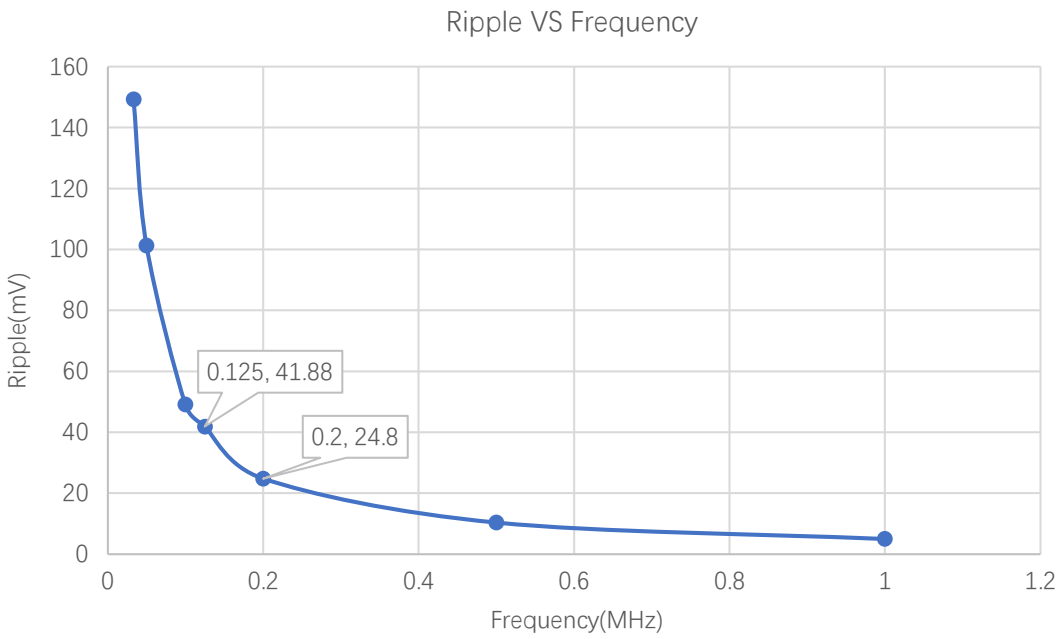


Figure 3.23: Ripple VS frequency

Moreover, clock frequency also influences the settling time. As shown in Equation 2.36, settling time is proportional to -V_{PP}:

$$T_{settling} \propto -V_{PP} \propto \frac{I_o}{fC_i} \tag{3.17}$$

When the loading current, capacitance in each stage, the number of stages keep constant, the settling time is inversely proportional to switching frequency, which is also shown in Figure 3.24.

Figure 3.24 shows the output voltage when the frequency is from 33.33 kHz to 1 MHz. It can be clearly seen that as the frequency increases, the output voltage stabilizes faster and faster, and the achievable amplitude becomes larger, but when the frequency increases further, the output voltage increment becomes smaller and smaller. When the frequency is infinite, the output voltage will stabilize at the output voltage value under no load condition. When frequency is chosen at 200 kHz, the circuit can stabilize within 272.6 us, reaching 3.20 V, which is 98% of the V_{out} of pss rms simulation.

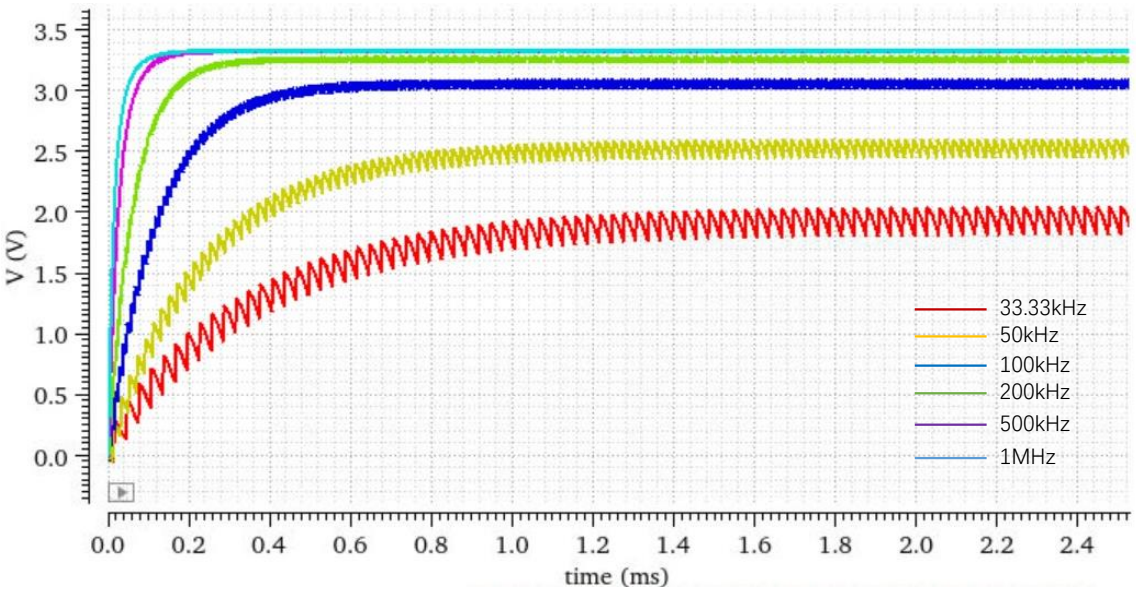


Figure 3.24: Settling time with different frequencies

3.6 Power efficiency optimization

The analysis of power consumption and capacitance selection earlier was based on a load current of 1 uA. However, the maximum efficiency that the circuit can achieve under different load conditions may vary, and there is a optimal loading current for the same ripple.

Since changing the load will also change the ripple, to keep the ripple consistent, the output capacitance is constant and the frequency is changed. The efficiency VS C_i curve with different loading current is shown in Figure 3.25.

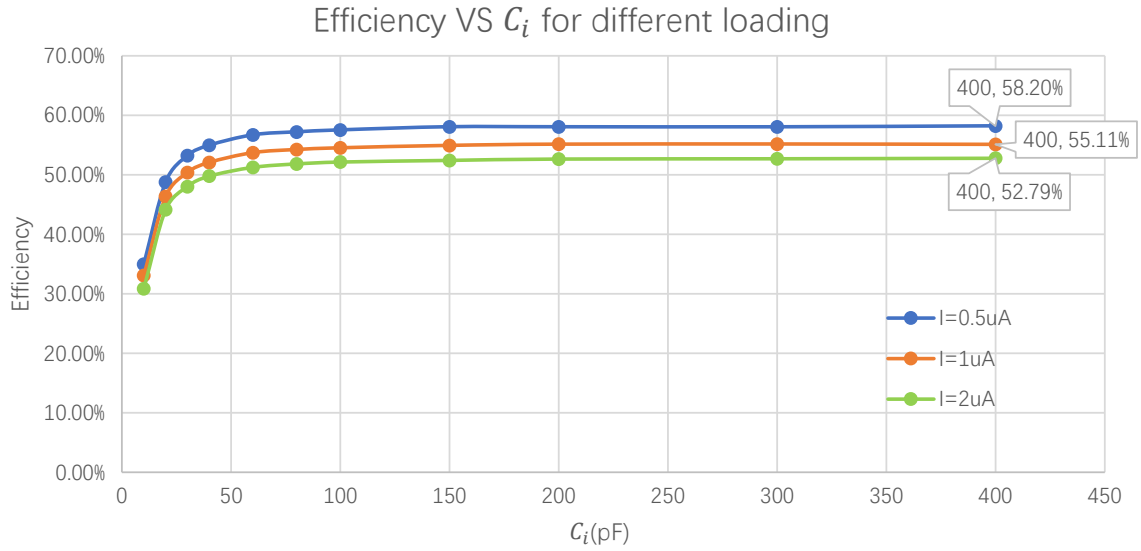


Figure 3.25: Efficiency VS C_i for different I_o

For each current load, the trend of power efficiency is similar to the analysis in the previous Figure 3.20. But the maximum power efficiency changes. Take a load of 0.5 uA for example, the maximum efficiency is58.2%, which is higher than 55.2% when loading current is 1 uA. This can be understood in two ways. One way is to analyze from the expression of efficiency Equation 3.8.

$$\frac{1}{\eta} = \frac{V_{DD} \cdot I_{in} + P_{buffer}}{V_{out} \cdot I_o} \tag{3.18}$$

As the power consumed in buffer can be divided into two parts: one part is the power consumption $P_{buffer,0}$ without loading ,which is constant; another part is the power related to the loading current, which can be written as

$$\Delta P_{buffer} = k \cdot I_{load} \cdot V_{clk} \tag{3.19}$$

k is a coefficient that is related to the capacitance C_i and parasitic capacitance, frequency and number of stages[31]. Then Figure 3.20 can be calculated:

$$\frac{1}{\eta} = \frac{V_{DD}}{V_{out}} + \frac{P_{buffer,0}}{V_{out} \cdot I_o} + \frac{k \cdot V_{clk}}{V_{out}} = E_1 + E_2 + E_3 \tag{3.20}$$

$E_1 = \frac{V_{DD}}{V_{out}}$, $E_2 = \frac{P_{buffer,0}}{V_{out} \cdot I_o}$ and $E_3 = \frac{k \cdot V_{clk}}{V_{out}}$. When increasing the loading current, V_{out} decreases, so E_1 and E_3 increases. The variation trend of E_2 depends on the combined effects of V_{out} and I_o. Figure 3.26 shows the relationship between V_{out} and I_o, which is calculated as

$$V_{out} = -0.33 \cdot 10^{-6} \cdot I_o + 3.6 \tag{3.21}$$

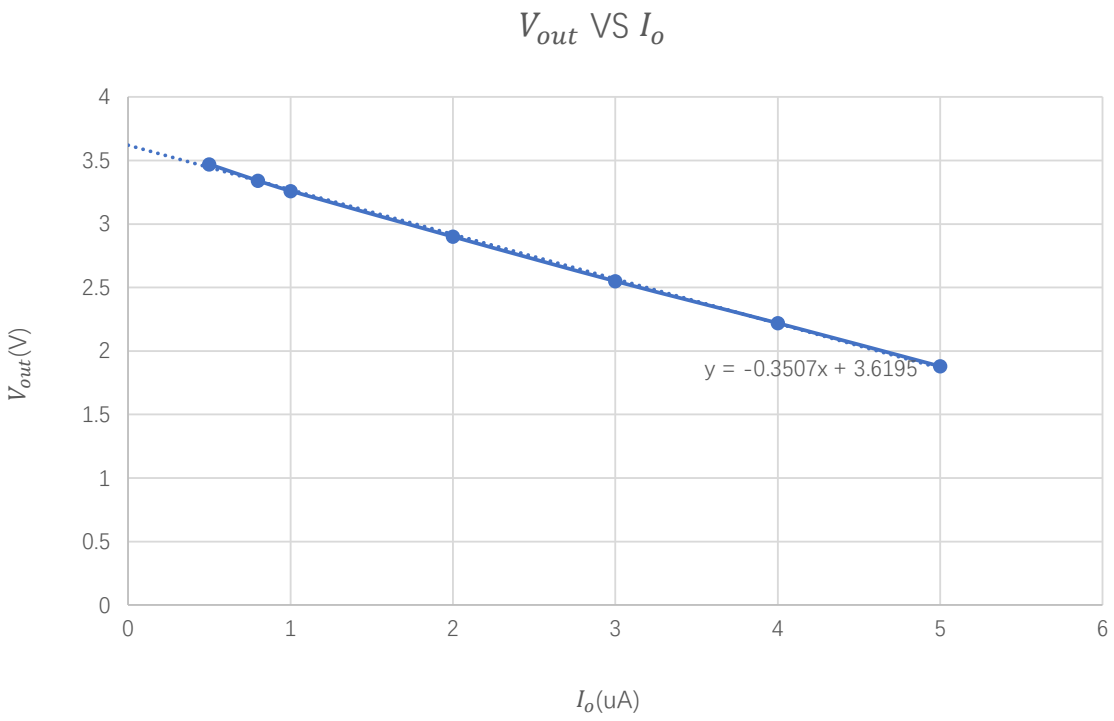


Figure 3.26: V_{out} with different I_o

So E_2 can be considered as inversely proportional to the loading current. Then in a certain range(when current is small), the increase in loading current is greater than the decrease in output voltage, so when the load current increases, E_2 decreases. The increase or decrease of $\frac{1}{\eta}$ depends on the relative values of the incremental changes in E_1 and E_3 and the decremental change in E_2. When the incremental changes in E_1 and E_3 are greater, the value of $\frac{1}{\eta}$ increases, resulting in a decrease in power efficiency. Therefore, under the condition of consistent ripple, an increase in load current will lead to a decrease in power efficiency, which is shown in Figure 4.24.

Another way to analyze power efficiency is discussed below. As power consumed on buffer can be divided into two parts: one part related to the loading current and another part consumed by the parasitic cap. For each stage, when clock signal is high, the charge transferred during one period Q is calculated as:

$$Q = I_o \cdot T \tag{3.22}$$

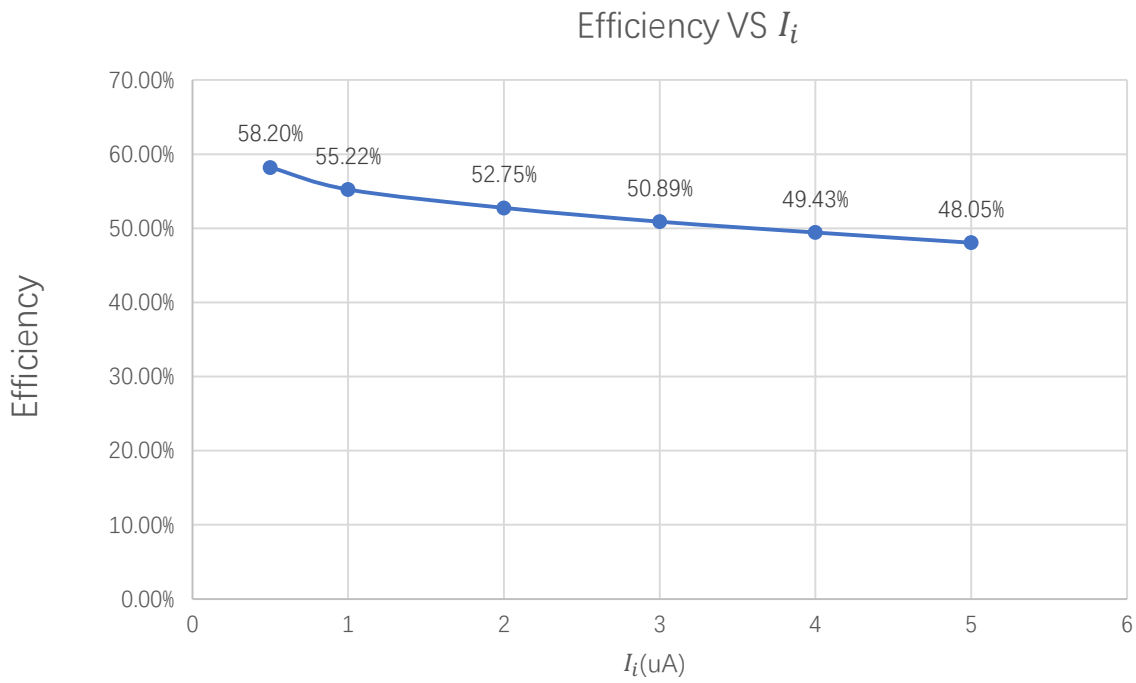


Figure 3.27: Maximum efficiency VS I_o with fixed ripple

Because only half of the period is charging time, so the average current flowing through the buffer in one stage is:

$$I_{avg} = \frac{Q}{T/2} = 2I_o \cdot T \tag{3.23}$$

Then the power consumed for one stage ignoring the parasitic capacitance is

$$P_i = I_{avg} \cdot V_{clk} = \frac{Q}{T/2} = 2I_o \cdot T \cdot V_{clk} \tag{3.24}$$

For a N-stage charge pump, only N/2 stages are charging at one period, so the total power consumed in buffer ignoring the parasitic capacitance is

$$P_N = N/2 \cdot I_{avg} \cdot V_{clk} = \frac{Q}{T/2} = N \cdot I_o \cdot T \cdot V_{clk} \tag{3.25}$$

Then the total power consumed by buffer can be written as:

$$P_{buffer} = N \cdot I_o \cdot T \cdot V_{clk} + c_p \cdot f \cdot V_{clk}^2 \tag{3.26}$$

where c_p is the parasitic capacitance of buffer and $c_p \cdot f \cdot V_{clk}^2$ the power consumed by c_p. Then Equation 3.8 can be written as

$$\eta = \frac{V_{out} \cdot I_o}{V_{DD} \cdot I_{in} + N \cdot I_o \cdot T \cdot V_{clk} + c_p \cdot f \cdot V_{clk}^2} \tag{3.27}$$

from which I_{in} equals to I_o.

When frequency is changed to keep ripple constant, Equation 3.27 can be derived to

$$\eta = \frac{V_{out}}{V_{DD} + N \cdot T \cdot V_{clk} + c_p \cdot V_{clk}^2 \cdot \frac{f}{I_o}} \tag{3.28}$$

The denominators are all constant terms, and as shown in 3.26, V_{out} is inversely proportional to I_o. So increasing loading current will contributes to a decrease in V_{out} as well as power efficiency.

When ripple is changed and frequency is constant, there will be optimal value of I_o. Equation 3.27 can be derived to:

$$\eta = \frac{1}{\frac{V_{DD}}{V_{out}} + \frac{N \cdot V_{clk}}{V_{out}} + \frac{f}{V_{out} \cdot I_o} \cdot C_b \cdot V_{clk}^2} \tag{3.29}$$

from which

$$V_{out} \cdot I_o = V_{DD} - N \cdot V_{th} + N(V_{clk} - \frac{I_o}{f \cdot C_i}) \cdot I_o \tag{3.30}$$

As Equation 3.30 has a maximum value during a current range, efficiency in Equation 3.29 has a maximum value. As shown in Figure 3.28, the optimal loading current in Dickson charge pump is 2 uA with an efficiency of 56.07%.

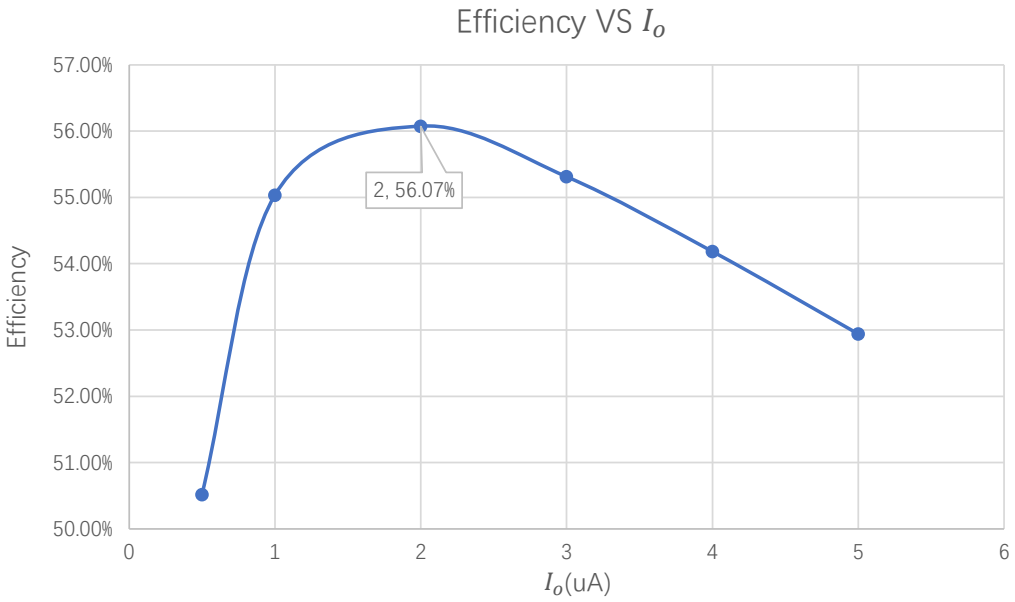


Figure 3.28: Maximum efficiency VS I_o with fixed frequency

3.7 Issue of Dickson

The Dickson charge pump, although simple in structure and easy to design, has two obvious drawbacks:

- The output voltage is limited by the CMOS threshold voltage. Due to the existence of the threshold voltage, more stages are needed to achieve the expected output voltage, which means larger area and more power consumption, resulting in higher costs and lower efficiency.
- The output current capability is limited. As simulated, with the load current increases, the maximum efficiency that the circuit can achieve decreases. In addition, to achieve maximum efficiency, a larger capacitance value is required, which means a larger area is needed as well.

In conclusion, the parameters designed in a 4-stage Dickson charge pump is shown in Table 3.2.

I_o	L	W	Ripple	Frequency	C_i	C_L	V_{out}	Area	η
1 uA	6 um	40 um	25 mV	200 kHz	60 pF	100 pF	3.26 V	0.061 mm^2	53.72%

Table 3.2: Parameters designed in Dickson charge pump

To overcome the issue of limited output voltage in Dickson charge pumps due to threshold voltage, [1] proposes a new topology that utilizes static charge transfer switches to achieve higher pumping voltage. The details will be discussed in Chapter 4.

4

Charge Pump with Charge transfer switches

4.1 The static CTS's

4.1.1 Principle of static CTS's topology

As discussed in Chapter 3, there is a threshold voltage drop in Dickson charge pump. More stages are needed to get the expected output voltage. To remove the threshold voltage drop in each stage, a new topology called Static Charge Transfer Switches(CTS's) is proposed in [1]. The schematic of this topology is shown in Figure 4.1.

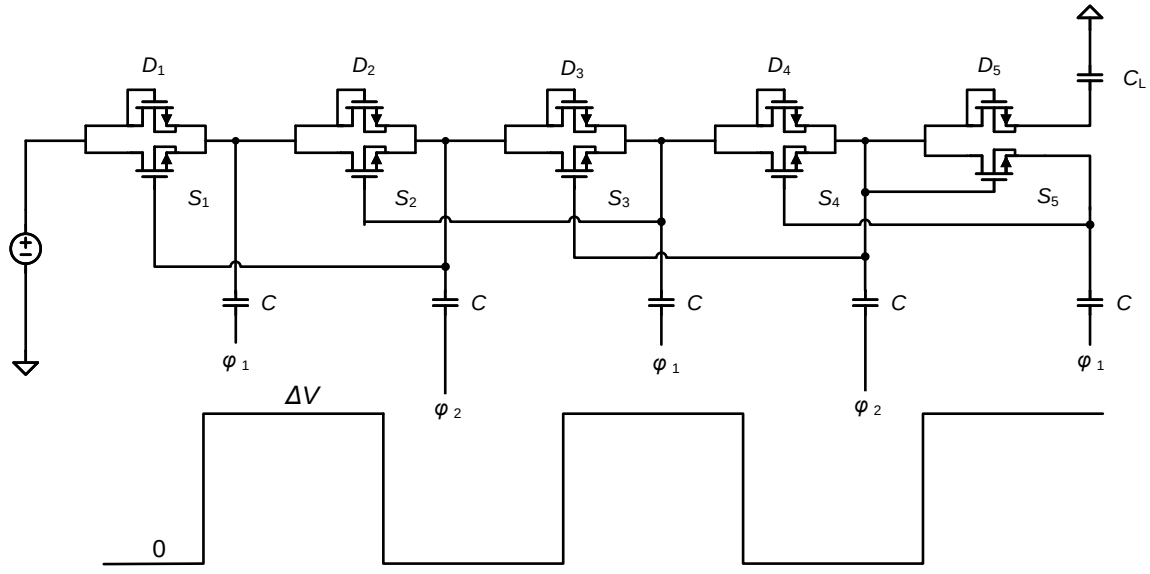


Figure 4.1: Schematic of charge pump with static CTS's

Compared to Dickson charge pump, a parallel MOSFET S_i is connected to the original MOSFET D_i in each stage. And the gate of the parallel MOSFET S_i is controlled by the voltage at next stage. The parallel switches help to charge V_i to the high voltage of V_{i-1} in steady state. In Dickson charge pump, the switch will be cut off when

$$V_{GS,D} < V_{th,D} \tag{4.1}$$

from which $V_{GS,D}$ is the voltage over gate terminal and source terminal of MOSFET diode(MD), and $V_{th,D}$ is the threshold voltage of MOSFET diode. Then the charging process stops and V_i will be equal to $V_{i-1} - V_{th}$. But in the new topology utilizing static CTS's, when the upper MOSFET works in cut-off

region, the below MOSFET switch will continue to charge the capacitor. As the difference between gate voltage and source voltage is the high stable voltage of V_i minus the low stable voltage of V_{i-1}, which is $2\Delta V$. If Equation 4.2 holds,

$$2\Delta V > V_{th,S} \tag{4.2}$$

the parallel switch S_i is turned on and keeps charging V_i to V_{i-1}. Then there is no limit of threshold voltage.

The dynamic changes of the voltages V_i are as the same as the situation in Dickson charge pump ignoring V_{th} in Figure 2.5. The ideal voltage's waveforms in stead state are shown in Figure 4.2.

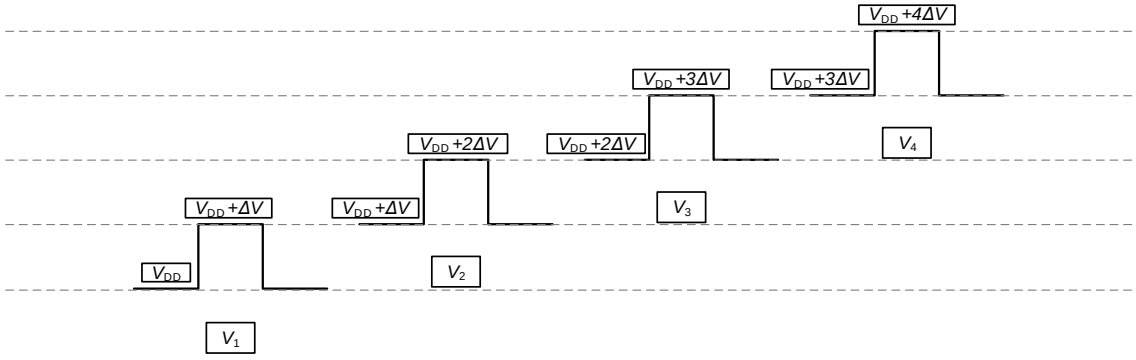


Figure 4.2: Voltages of charge pump with static CTS's

Assume all the initial node voltages are 0, all the capacitors can be charged and discharged completely in a very short time. Take the first stage for example to analyze:

- t = 0. ϕ_1 is low and ϕ_2 is high, D_1 is turned on. V_1 is charged by the voltage source to $V_{DD} - V_{th}$, V_2 is raised to ΔV by the clock signal. The voltage over gate terminal and source terminal of S_1 V_{GS} is smaller than threshold voltage of S_1, so S_1 will keep open.
- t = $\frac{T}{2}$. ϕ_1 is high and ϕ_2 is low, D2 is turned on. V_1 is pulled up to $V_{DD} - V_{th} + \Delta V$. V_2 is pulled down to 0 firstly, and then is charged by C_1 through D_2 to $V_{DD} - 2V_{th} + \Delta V$. $V_{GS} = -2V_{th} + \Delta V$, if V_{GS} is smaller than V_{th}, S_1 keeps open.
- t = T. ϕ_1 is low and ϕ_2 is high, D_1 is turned on again. V_1 is pulled down to $V_{DD} - V_{th}$ at first, and V_2 is pulled up to $V_{DD} - V_{th} + 2\Delta V$. At this time, V_{GS} of S_1 is $-V_{th} + 2\Delta V$, which is larger than V_{th}, so S_1 will be turned on. Then the voltage source will continue to charge C_1 through S_1 to V_{DD}.

When circuit works in steady state, voltage in i^{th} stage stabilize between $V_{DD} + (i-1) * \Delta V$ and $V_{DD} + i * \Delta V$. The threshold voltage drop of MOSFET has been removed.

Take stable state of the first stage for example to analyze the charging process. When V_1 is low, D_1 is turned on, and V_{DD} will charge V_1 to $V_{DD} - V_{th}$. At this time, V_2 is at high voltage, with a value of $V_{DD} + 2\Delta V$. So the voltage between gate and source of MOSFET switch S_1 is $2\Delta V$, which turns on S_1. Then V_{DD} continues to charge V_1 from $V_{DD} - V_{th}$ to V_{DD} through S_1.

4.1.2 Potential risks of static CTS's topology

Although the static CTS structure can eliminate the limitation of threshold voltage, it has a fatal issue, which is the problem of reverse charge sharing. The voltage drop over the gate terminal and source terminal of S_i is always $2V_{clk}$. When the clock in i^{th} stage is low, to make V_i equal to the high voltage of the previous stage, S_i needs to be turned on, and Equation 4.3 needs to be satisfied.

$$V_{GS} = 2\Delta V > V_{th,S} \tag{4.3}$$

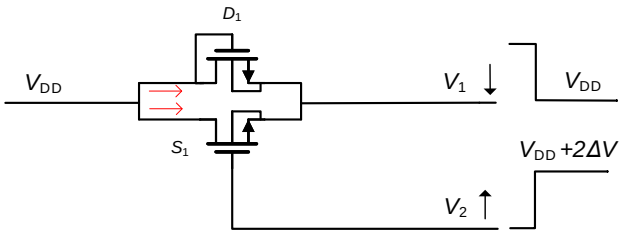


Figure 4.3: MS is on

Compared with the conduction condition $\Delta V > V_{th,D}$ of the Dickson charge pump, the charge pump based on static CTS's is more suitable for low supply voltage applications.

When the clock signal in i^{th} stage is high, the switch S_i is expected to be turned off. Otherwise, due to the voltage difference, the i^{th} level will reverse charge the previous level. In steady state, V_{GS} also equals to $2\Delta V$, which should be lower than the threshold voltage to cut off the switch, meaning that Equation 4.4 must be satisfied.

$$V_{GS} = 2\Delta V < V_{th,S} \tag{4.4}$$

It can be clearly seen from Equation 4.3 and Equation 4.4 that these two equations cannot be satisfied at the same time. In order to meet the charging condition, the switch cannot be completely closed in the other half cycle when it should be closed. This is why the phenomenon of reverse charge sharing will occur, which is manifested as a voltage drop. Figure 4.4 shows the simulation results of a 4-stage static CTS's structure.

For a four-stage static CTS's charge pump,the output voltage is 3.5 V when there is no load, which is smaller than 4.24 V in Dickson charge pump. As can be seen in Figure 4.4. When V_2 is charging V_3, even when V_2 is equal to V_3, V_2 will continue to discharge and not stabilize because the switch cannot completely turn off, resulting in reverse charging of the charge. The continuous increase in voltage of V_3 is due to V_4 reverse charging V_3. In order to solve the problem of reverse charge sharing, another new topology is introduced, which will be discussed in detail in Section 4.2.

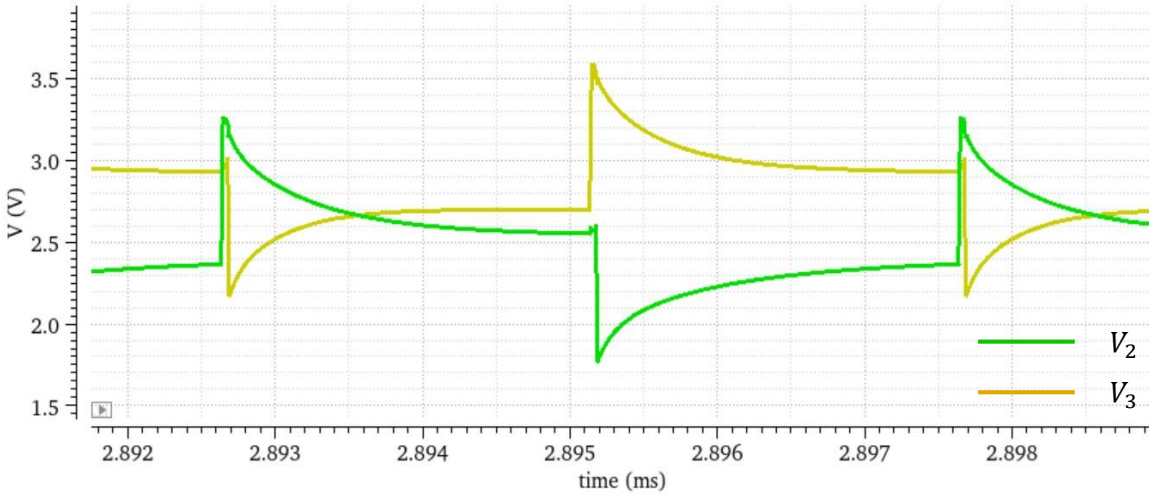


Figure 4.4: Simulation results of V_2 and V_3 in static CTS's charge pump

4.2 The dynamic CTS's

For the static CTS's charge pump structure, there will be an obvious phenomenon of reverse charge sharing because the transistors cannot be turned off during the time when the voltages at the bottom plate of the capacitors C_i are pulled down. Therefore, topology of charge pump utilizing dynamic CTS's is proposed in [1]. This new topology introduces inverters to dynamically control the switching state of the transistors.

4.2.1 Principle

The schematic diagram of the dynamic charge transfer switches(CTS's) is shown in Figure 4.5.

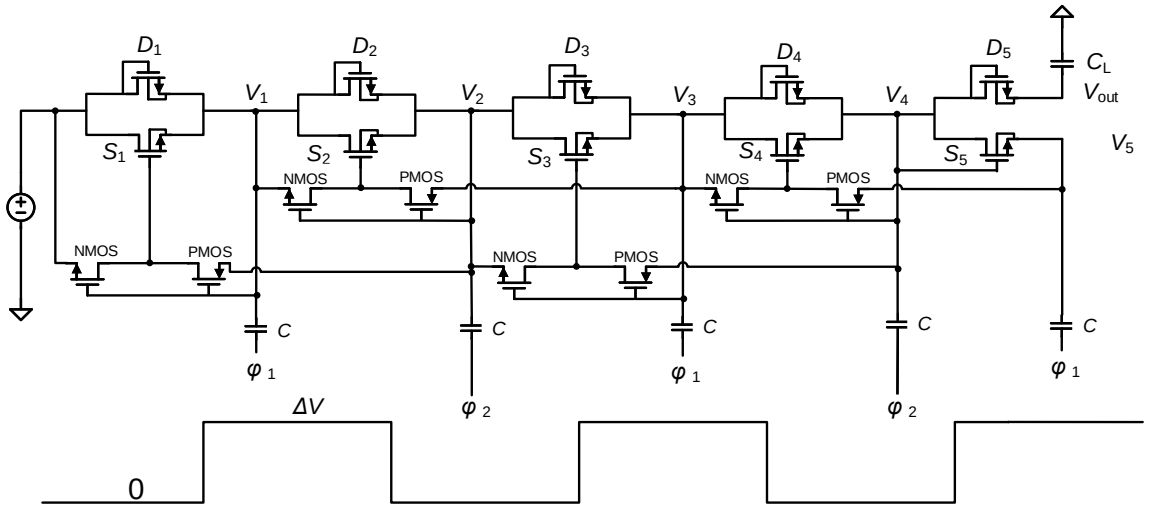


Figure 4.5: Schematic of dynamic CTS's charge pump

Take the second stage for example to analyze the working process. The gate terminal of the inverter is connected to V_2, the source terminal of the NMOS is connected to V_1, and the source terminal of the PMOS is connected to V_3. The drain terminal of both the NMOS and the PMOS, which is the output of the inverter, is connected to the gate terminal of the MOS switch.

- When ϕ_2 is low, shown in Figure 4.6a, V_2 is at the low voltage of $V_{DD} + \Delta V$, V_1 and V_3 are at high voltages, which are $V_{DD} + \Delta V$ and $V_{DD} + 3\Delta V$, respectively. At this moment,

$$V_{GS,n} = V_2 - V_1 = 0 < V_{th,n} \tag{4.5}$$

$$V_{GS,p} = V_2 - V_3 = -2\Delta V < -V_{th,p} \tag{4.6}$$

  So the PMOS is turned on and NMOS is turned off. Then the gate voltage of MOS switch S_2 V_{g2} equals to V_3, which is $V_{DD} + 3\Delta V$. When $V_{GS,S2}$ is greater than $V_{th,S}$, MOS switch S_2 turns on, and the voltage of V_2 is charged from $V_1 - V_{th}$ to V_1 through S_2 .

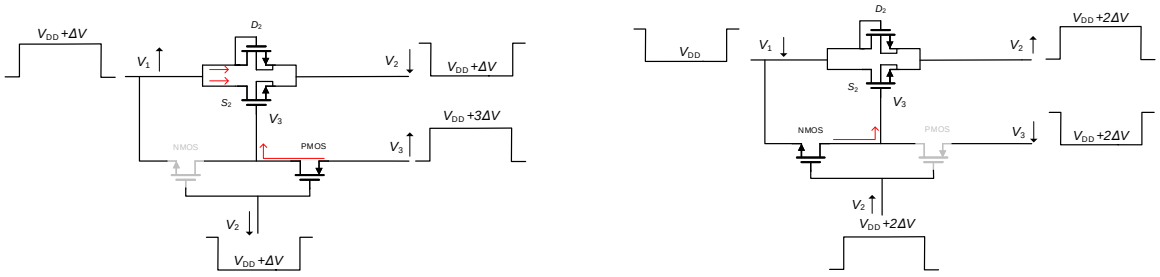
- When ϕ_2 is high, shown in Figure 4.6b, V_2 is at the high voltage of $V_{DD} + 2\Delta V$, and V_1 and V_3 equals V_{DD} and $V_{DD} + 2\Delta V$, respectively. Then

$$V_{GS,n} = V_2 - V_1 = 2\Delta V > V_{th,n} \tag{4.7}$$

$$V_{GS,p} = V_2 - V_3 = 0 > -V_{th,p} \tag{4.8}$$

  So the NMOS is turned on and PMOS is turned off. Then output voltage of the inverter is V_{DD}, which cause $V_{GS,S2} = 0$. The MOS switch S_2 be can turned off.

The introduction of the inverter can dynamically turn off the charge transfer switch during the clock's blocking period and turn it on during the time when the voltages at the bottom plate of the capacitors



(a) Situation when PMOS is 'ON'

(b) Situation when NMOS is 'ON'

Figure 4.6: Two states of the second stage

C_i are pulled up. From Equations 4.6 and Equations 4.7, it can be concluded that the working condition of the dynamic CTS structure is

$$2\Delta V > (V_{th,n}, V_{th,p})_{max} \tag{4.9}$$

4.2.2 Design considerations

For dynamic CTS's structure, area occupation, power consumption, and ripple should be considered comprehensively in the design process. In this subsection, the selection of component sizes will be specifically discussed.

4.2.2.1 MOSFET diode design

The size design of MOSFET that works as diode is similar to the situation in Dickson charge pump. When the circuit is loaded with a 1 uA current, and the clock frequency is 200 KHz, the relationship between the output voltage of a 4-stage charge pump and the channel length is shown in the Figure 4.7, with the 'aspect ratio' of the MOSFET diode kept at a value of 5/2.

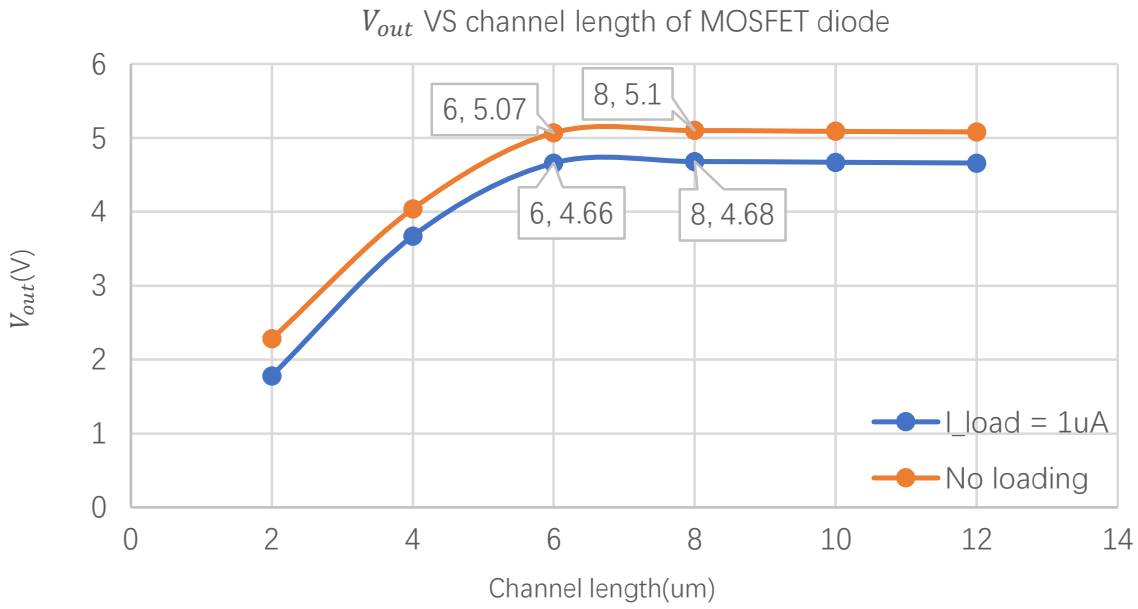


Figure 4.7: V_{out} VS channel length of MOSFET diode

When the channel length is short, the presence of leakage current will result in a small output voltage.

From the data, it can be seen that when the channel length is greater than 6 um , there is no much gain by increasing the channel length to achieve higher output voltage level. Therefore, channel lengths ranging from 6 um to 12 um can be considered as optimal values. When L=8 um, the output voltage is at its highest value, so the selected channel length for MOSFET diode is 8 um.

Once the length is determined, the transistor size can be changed by altering the width while keeping the length constant. The graph showing the change in output voltage as a function of MOSFET width is depicted as Figure 4.8.

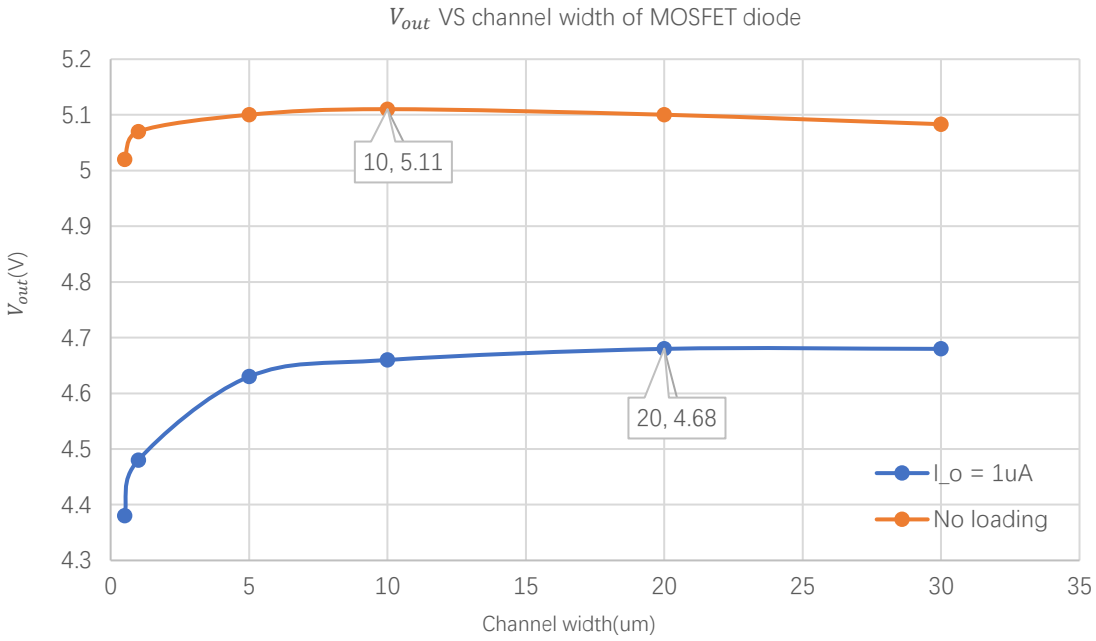


Figure 4.8: V_{out} VS channel width of MOSFET diode with a length of 8 um

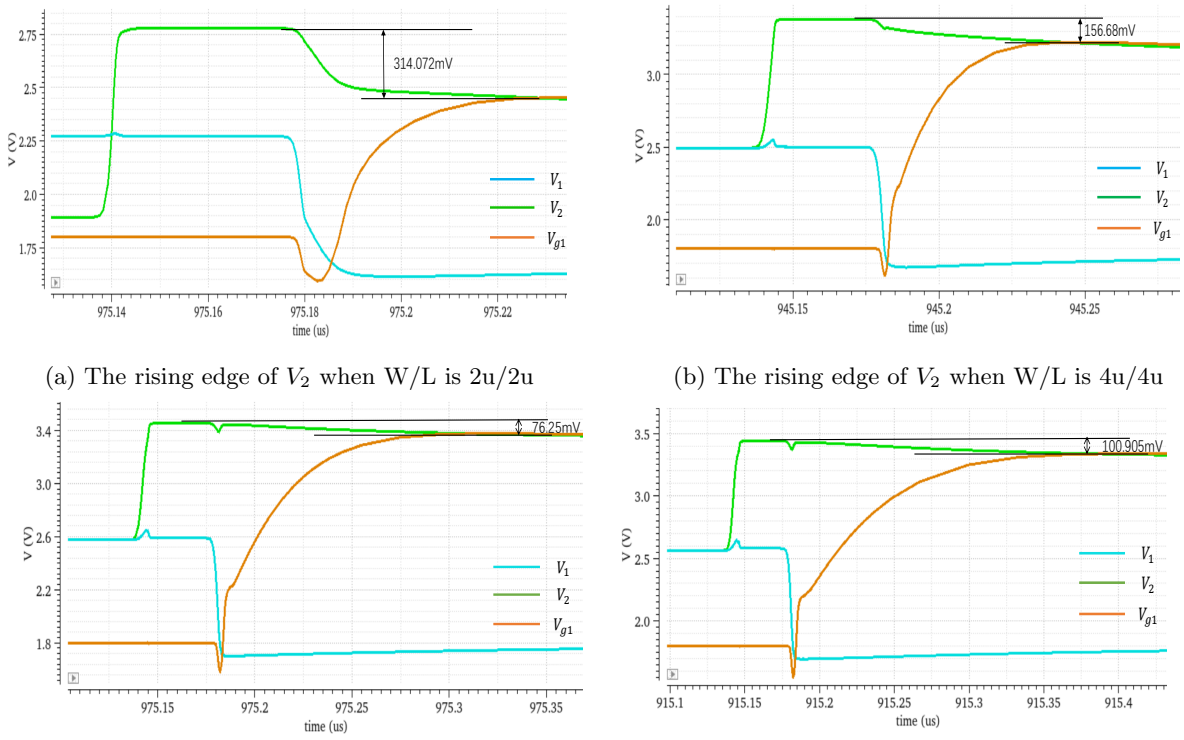
Small transistor need large V_{GS} to provide the same amount of current,leading to low output voltage. When the width is larger than 10 um, the increase in output voltage is only a few millivolts. So a width larger than 10 um are all optimal choice. To achieve the largest output voltage and small size, 20 um is chosen.

4.2.2.2 MOSFET switch design

Length The size of MOSFET switch MS is closely related to the inverter. When designing the channel length, the main consideration is leakage current. When ϕ_2 is high, MS2 should be in the off state, but due to the fact that V_2 is greater than V_1 at this time, the V_{ds} of MS2 is $V_2 - V_1$, and the transistor cannot be completely turned off.There is a leakage current from V_2 to V_1, which reduce the level of V_2. To increase the resistance of MS in the off state, the channel length should be increased.

Figure 4.9a, Figure 4.9b and Figure 4.9c Figure 4.9d indicate the output voltage for 'aspect ratio' of 1/2 and channel lengths of 2 um, 4 um, 6 um and 8 um. In Figure 4.9a, the leakage cause a large voltage drop of 314.072 mV, and the low voltage of V_2 can not even follow the high voltage of V_1. For channel lengths of 4 um, 6 um and 8 um, the voltage drops caused by leakage current in V_2 are 156.68 mV, 76.25 mV and 100.905 mV respectively, and it is clearly visible from the graph that in both cases, the low voltage of V_2 can follow the high voltage of V_1 well.

From Figure 4.9, 6 um is the optimal value of channel length. When the channel length is larger than 6 um, from the voltage drop of V_2, it can be seen that increasing the channel length further will not significantly enhance the suppression of leakage current, and V_2 decreases more. It's because of the parasitic capacitance in gate terminal $C_{p,g}$. To prove the effect of parasitic capacitance, a capacitor is



(a) The rising edge of V_2 when W/L is 2u/2u

(b) The rising edge of V_2 when W/L is 4u/4u

(c) The rising edge of V_2 when W/L is 6u/6u

(d) The rising edge of V_2 when W/L is 8u/8u

Figure 4.9: Drop of V_2 for different W/L

connected parallel to the gate terminal of MOSFET. Assume C_{ox} is about 10 fF,

$$C_{p,G} = C_{ox} \cdot W \cdot L \tag{4.10}$$

When W/L is 6 um/6 um, $C_{p,g}$ is calculated as 0.36 pF. Then a capacitance with a value of 0.3 pF is connected to the gate of transistor. The simulation results is shown in Figure 4.10. Drop on V_2 is 110.038 mV, which is close to the situation where W/L is 8 um/8 um. conclusion can be drawn that when channel length is smaller than 6 um,the effect of leakage current dominates; when channel length is larger than 6 um, the effect of parasitic capacitance dominates. So a length of 6 um is designed.

Figure 4.11 shows the relationship between output voltage and channel length of switch, which also indicates the fact that a channel length of 6 um is optimal.

Width The width of transistors can not be too small. Because small transistor need large V_{gs} to provide the same amount of current. If the width is too large, the parasitic capacitance will be large, then C_i needs to share more charges to the parasitic capacitance, which would lead to a smaller ΔV. If a large width is designed, large C_i can solve this problem. But large C_i also increase the area. Figure 4.12 shows the relationship between V_{out} and channel width of MOSFET switch.

When no load is applied, no load current will limit the minimum value of the transistor size, so for a smaller area, the width can take a minimum value of 0.5 um. When a loading current of 1 uA is applied, the channel width that can leads to the maximum V_{out} is 2 um. So a length of 6 um and a width of 2 um is chosen.

At steady state, when ϕ_1 transitions from low to high, the changes in V_1, V_2, V_3 and V_{g1} are shown in the Figure 4.13. To explain the waveform of the voltage in steady state shown in the Figure 4.13, the detail of the parasitic capacitances of a PMOS are shown in the Figure 4.14. C_{GS} is the parasitic capacitance between gate and source terminal, C_{GD} is the parasitic capacitance between gate and drain terminal and C_{DS} is the parasitic capacitance between drain and source terminal. For NMOS, there is also parasitic capacitances inside and the definition is similar.

There is a time difference of 40 ns between the rising edge of ϕ_1 and the falling edge of ϕ_2. When ϕ_1 is low, V_1 is equal to the power supply voltage V_{DD}, and V_2, V_{g1}, and V_3 are all equal to $V_{DD} + 2\Delta V$.

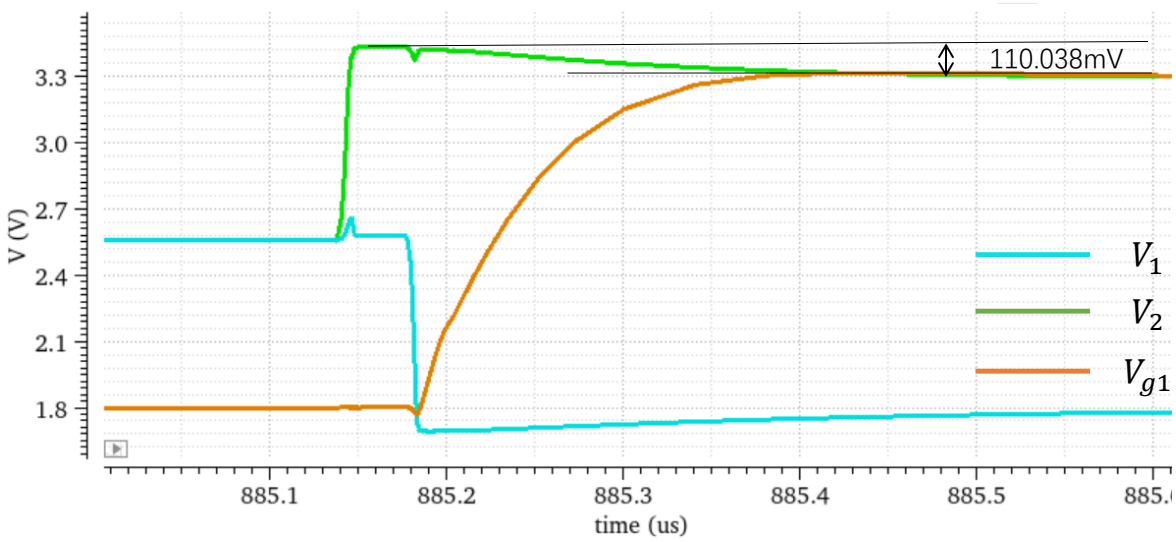


Figure 4.10: Drop of V_2 when a parallel cap added

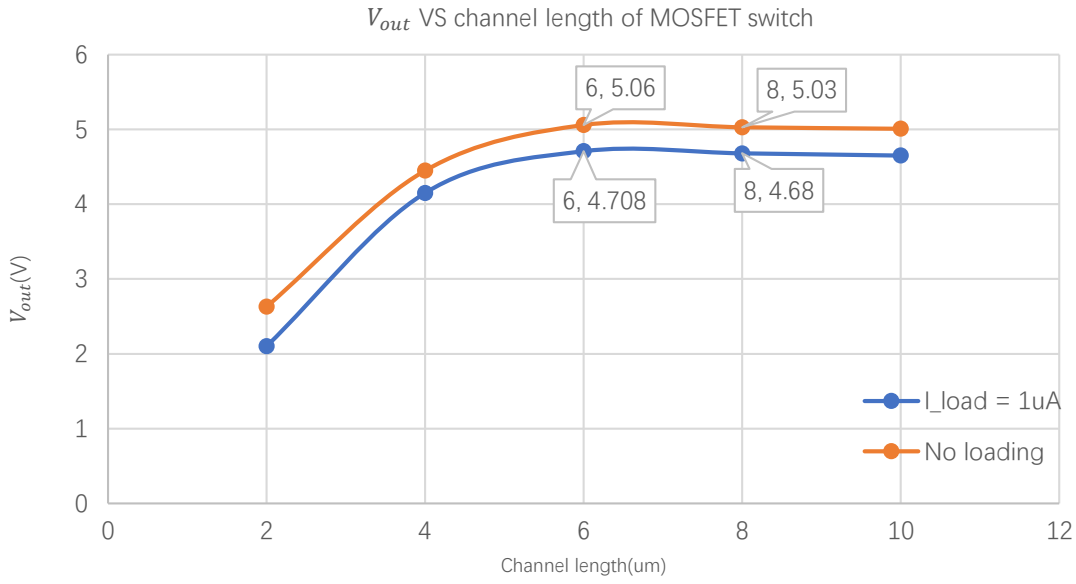


Figure 4.11: V_{out} VS channel length of MOSFET switch

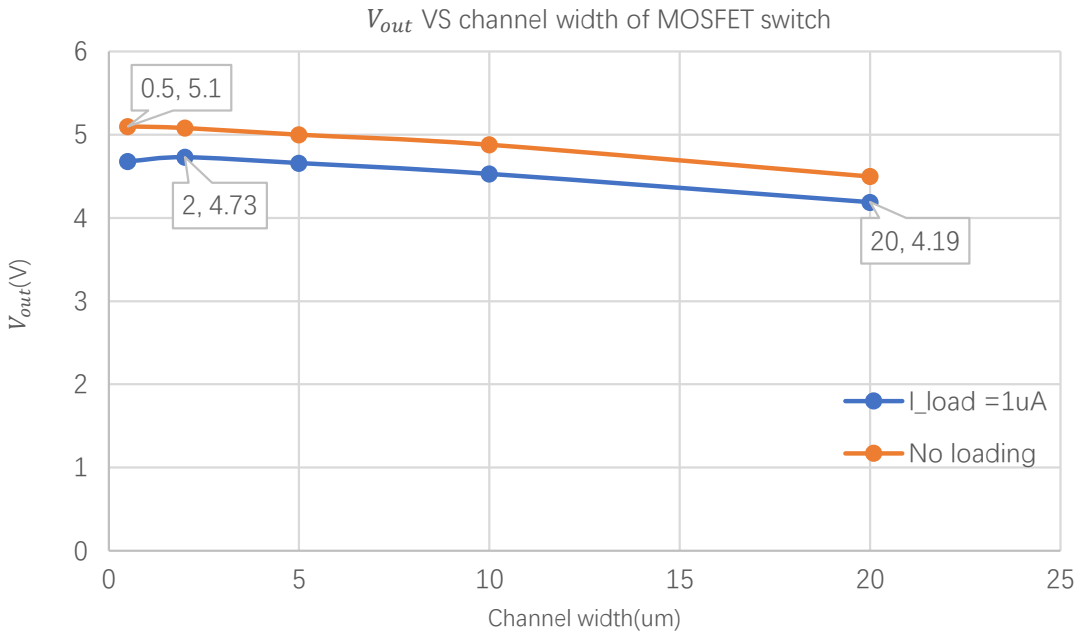


Figure 4.12: V_{out} VS channel width of MOSFET switch with a length of 6 um

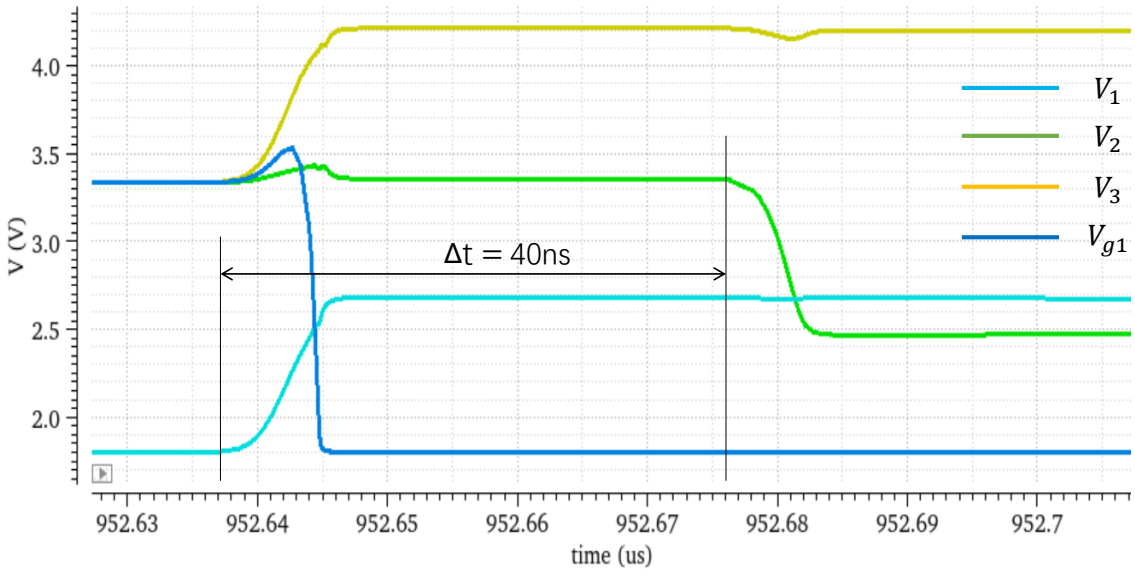


Figure 4.13: Voltages at falling edge of V_2 when W/L is 2u/6u

When the rising edge of ϕ_1 arrives, V_1 and V_3 are raised by the clock signal by ΔV, while V_2 and V_{g1} have small spikes in their waveforms, respectively due to the parasitic capacitance C_{GS} of the PMOS gate and source, and the parasitic capacitance C_{GD} of the NMOS and PMOS gates and drains shown in Figure 4.14.

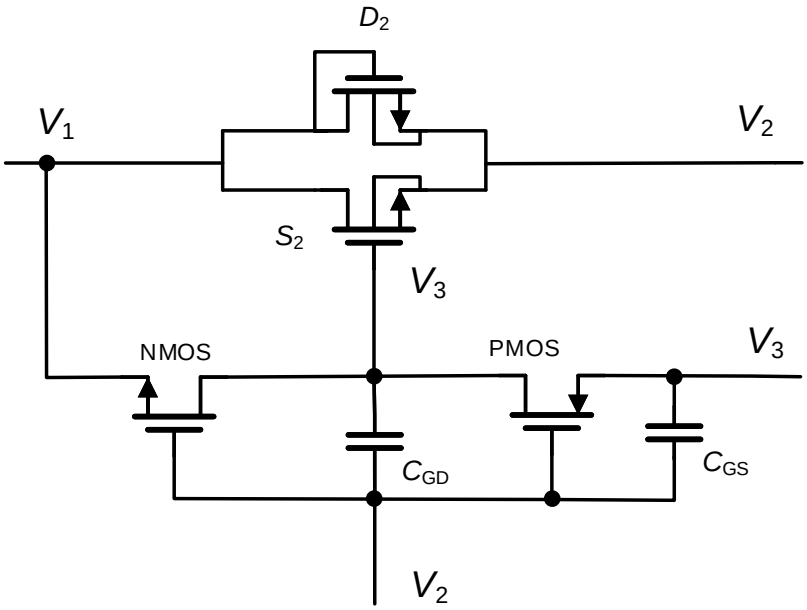


Figure 4.14: Parasitic cap inside MOSFET

Afterward, V_{g1} drops back to V_{DD} because the rising of V_1 turns on the NMOS. The voltage of V_2 will then decrease due to the parasitic capacitance C_{DS} between the drain and source, which pulls down V_2 as V_{g1} decreases. However, the clock signal for V_2 is still high at this time, so the clock signal keeps V_2 at a high voltage until the falling edge of ϕ_2 arrives.

When the falling edge of ϕ_2 arrives, V_2 is pulled low, and V_3 is also pulled low due to the parasitic capacitance C_{GD} of the PMOS. Then, the high clock signal charges V_3 back up to a high voltage. Afterwards, V_1 charges V_2, and finally, the voltages of both become the same.

4.2.2.3 Inverter design

An inverter is composed of a NMOS and a PMOS. Because the circuit requires different driving capabilities for PMOS and NMOS, there is no need to design the inverter as a symmetric structure.

NMOS For the design of the NMOS, the main requirement is that the switching speed needs to be fast enough. Taking the second stage as an example, when ϕ_2 is high, V_2 is $V_{DD} + 2\Delta V$, and the NMOS is turned on, V_{g2} is equal to V_1, which is equal to V_{DD}. Then MS2 is turned off, and V_2 remains at a high voltage. In this process, since the opening of the NMOS is controlled by the rise of V_2, the opening of the NMOS will be slower than the rise of V_2. There will be a time when V_2 is raised, during which MS2 is still conducting. Since V_2 is higher than V_1, charge will flow back to V_1 through MS2 in reverse resulting in a voltage drop at V_2.

In order to avoid the phenomenon of reverse charging, it is necessary to prevent the situation where MS2 is conducting when V_2 is at a high voltage. However, it is not possible to completely avoid this scenario. Therefore, the speed of the NMOS switch must be fast enough to quickly pull down V_{g2} , thereby rapidly turning off MS2 and reducing the time for reverse charging of the charge. Therefore, the NMOS driving capability needs to be strong , which means that the NMOS needs to be large in size.

Figure 4.15 indicates the V_{g2} over different NMOS size. As the size of the NMOS transistor decreases, when ϕ_2 is high, the V_{g2} voltage decreases more slowly. This implies that the switching speed of the NMOS transistor becomes slower.

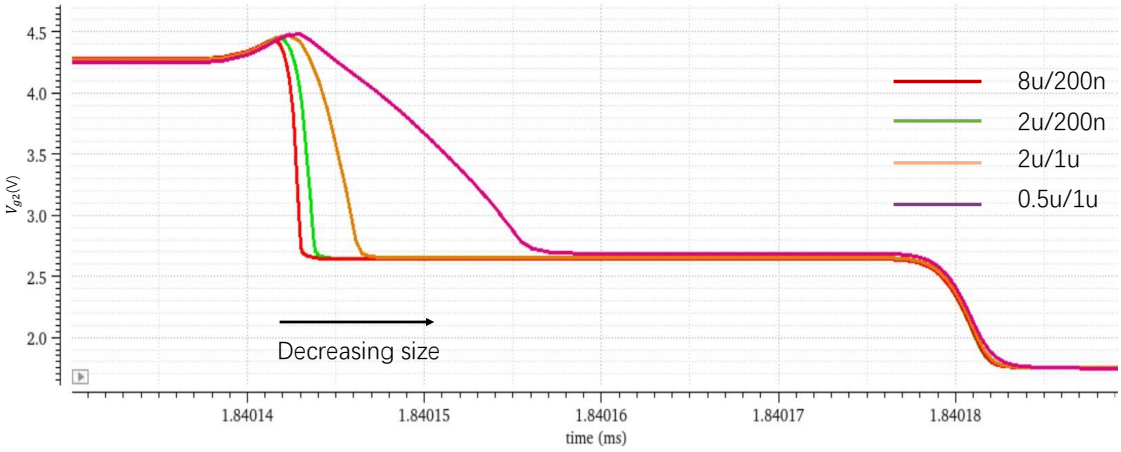


Figure 4.15: Different size of NMOS inverter

Figure 4.16 illustrates two scenarios where the NMOS sizes are 8um/220nm and 0.5um/2um respectively.

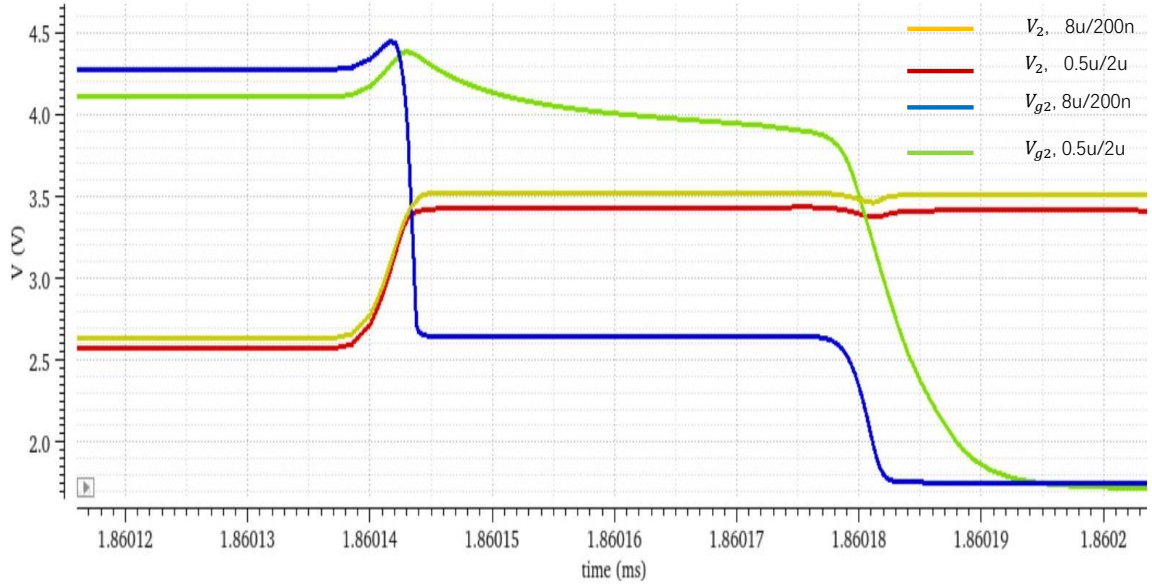


Figure 4.16: Large and small size of NMOS in inverter

When the NMOS size is 0.5um/2um, after the falling edge of the clock signal ϕ_1 arrives, V_{g2} remains high. This means that the switch MS2 remains conducting while both V_2 and V_1 are at high voltage. Even after V_1 transitions to a low voltage, MS2 continues to conduct, facilitating the movement of charges from the high voltage point V_2 to the low voltage point V_1. Therefore, when the NMOS transistor is of smaller size, the voltage difference ΔV at V_2 shown in the graph decreases by approximately 20mV.

In summary, the statement describes how a smaller NMOS size affects the V_{g2} voltage and the speed of the NMOS switch. Additionally, it explains the behavior of the MS2 switch and the movement of charges between V_2 and V_1 in the context of different voltages applied.

PMOS The PMOS mainly controls the charging process of V_2, so there is no need to make the PMOS switch very fast. It is only necessary to charge V_2 to $V_{DD} + 2\Delta V$ within the pumping period. On the

contrary, when the switch speed is too fast, it will decrease the output voltage. The reason is that when the driving capability of the PMOS transistor is enhanced, the driving capability of the NMOS transistor will be relatively weaken, resulting in a decrease in the output voltage. Figure 4.17 shows the voltages in different size of PMOS. Finally, the size of 1.335 um/8 um is chosen.

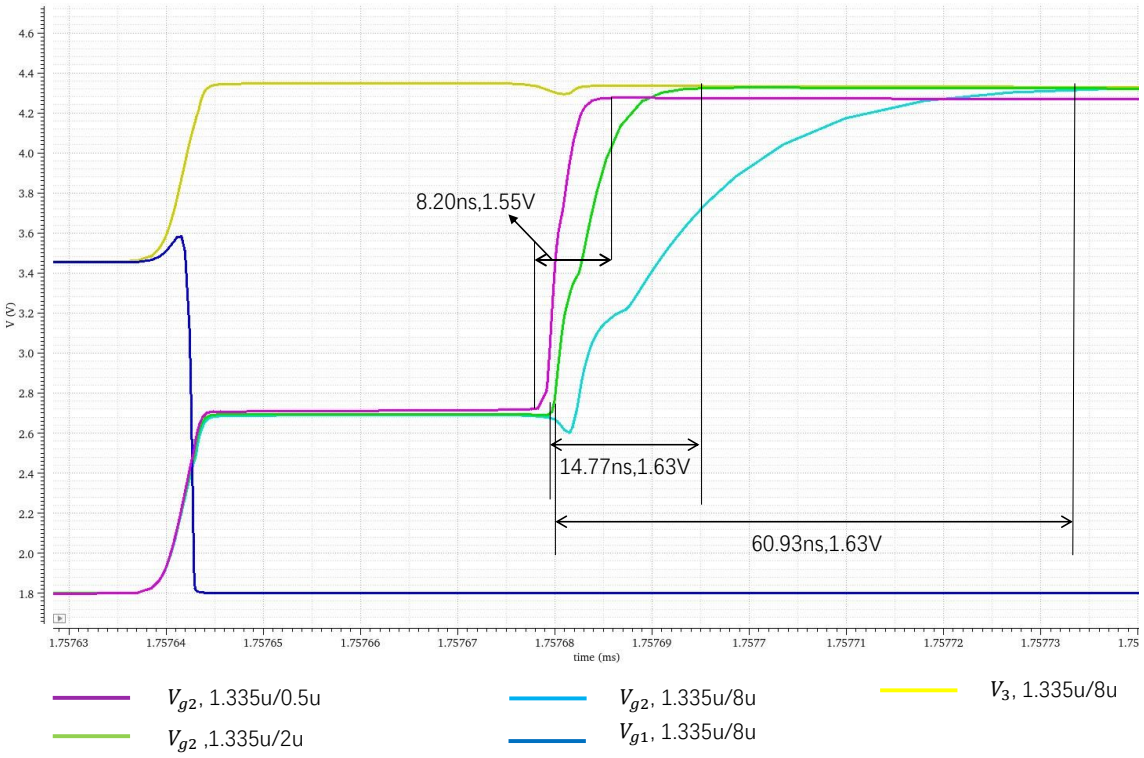


Figure 4.17: Different size of pmos in inverter

4.2.2.4 Area limitation

Compared to the Dickson charge pump, the charge pump structure that utilizes dynamic charge transfer switches has two additional cells for each stage. The MOSFET cell that works as a switch and the inverter consists of a PMOS and a NMOS. Figure 4.18 shows the layout diagram of the diode-connected MOSFET. In order to achieve the desired length of 8 um, four identical NMOS transistors with a channel length of 2um need to be connected in series. Each transistor has a finger length of 1 um, with a total of 20 fingers, resulting in a total width of20 um. Therefore, the area of each stage connected by diode-connected MOSFET shown in Figure 4.18 is 669.9 um^2.

Figure 4.19a shows the layout diagram of the MOSFET switch, whose 'aspect ratio' is 2 um / 6 um, comprised of three MOSFETs connected in series, each with a size of 2 um / 2 um. The area of the switch is calculated as 59.62 um^2.

Figure 4.19b depicts the layout of inverter in each stage. The inverter is designed with an NMOS width of 8 um and length of 200 nm, while the PMOS size W/L is 1.335 um / 8 um. The PMOS is constructed by serially connecting four transistors, each with a length of 2 um. Considering the inverter as a cell, the occupied area of the inverter, as shown in Figure 4.19b, is 100.37 um^2.

And the buffer designed in dynamic CTS's charge pump is as the same as that in Dickson charge pump, whose area is 37.71 um^2. As discussed in Chapter 3, the capacitance density $C_{density}$ is 5.604 fF/um^2. So the capacitance with a value of 60 pF occupies an area of 10 706 um^2. In each stage, the total area occupied by devices other than capacitors is denoted as

$$A_{diode} + A_{switch} + A_{inverter} + A_{buffer} = 669.9 + 59.62 + 100.37 + 37.71 = 867.6um^2 \ll 10706um^2 \quad (4.11)$$

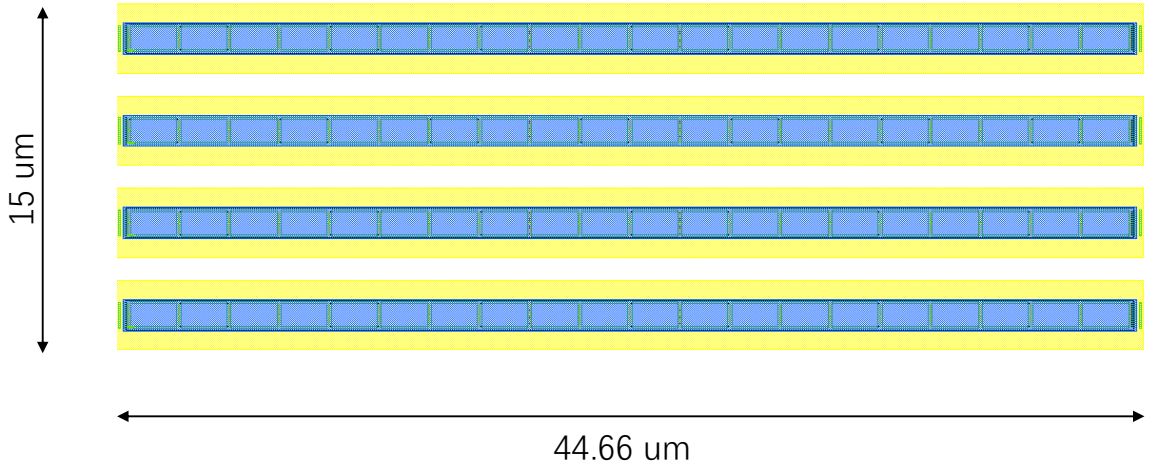
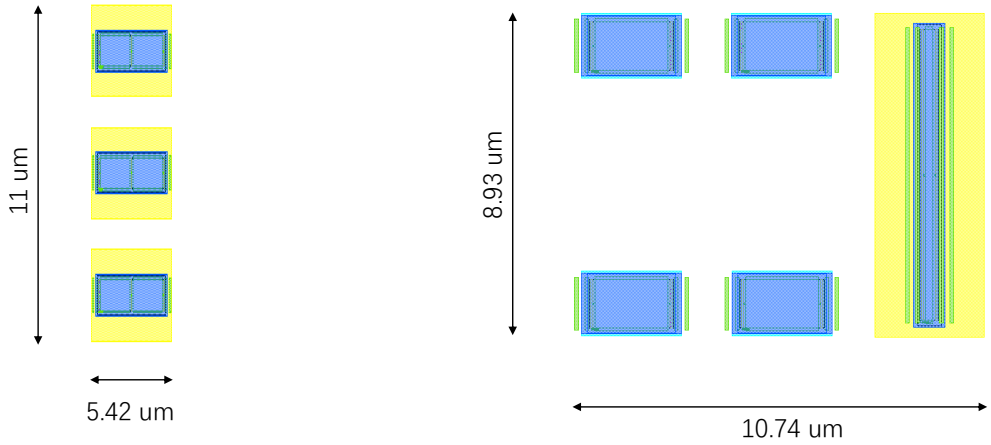


Figure 4.18: Layout of diode-connected CMOS



(a) Layout of MOSFET switch

(b) Layout of inverter

Figure 4.19: Layout of MOSFET switch and inverter

which is significantly smaller compared to the area occupied by capacitors, denoted as 10 706 um^2. Therefore, when calculating the total area occupied by the circuit, it is still approximately calculated using Formula 4.12.

$$Area = \frac{NC_i + C_L}{C_{density}} \tag{4.12}$$

4.2.2.5 Capacitance choice

When loading current is 1 uA, the total area needed according to different range of C_i is shown in Figure 4.20. The area and capacitance have a generally linear relationship, indicating that smaller capacitance is preferable in terms of area efficiency. Then the relationship between efficiency and C_i is discussed.

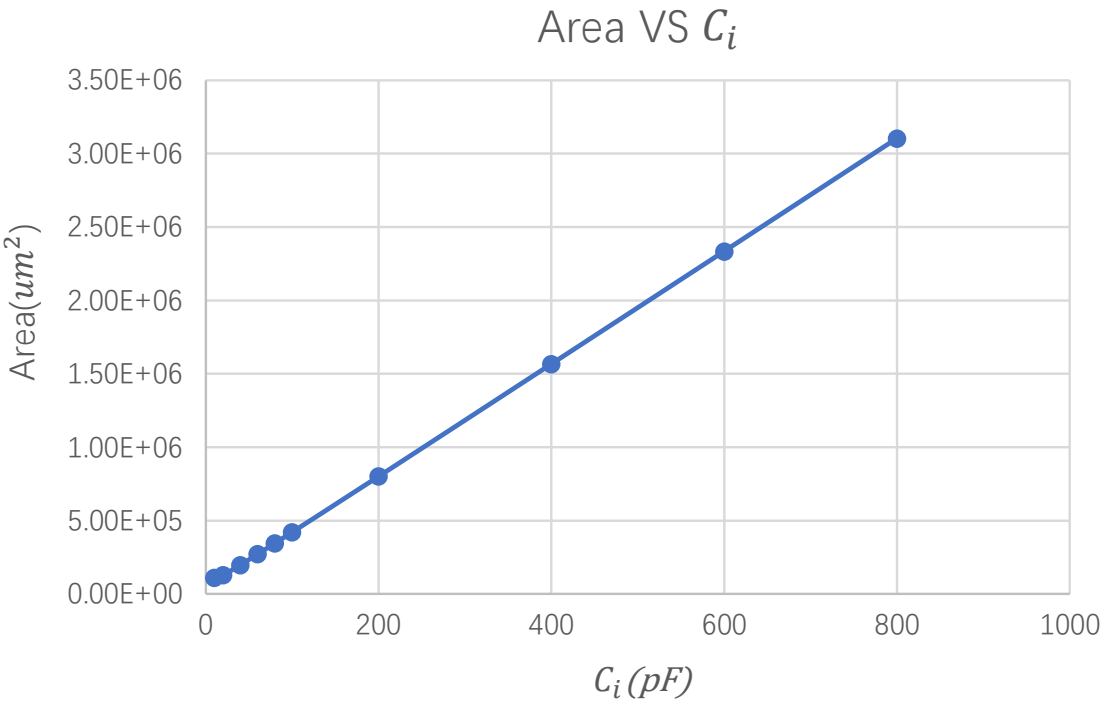


Figure 4.20: Area VS C_i

Figure 4.21 indicates the relationship between efficiency and C_i. The trend is similar to the analysis in section3.4.1. When the capacitance is small, efficiency increases with increasing capacitance because the output voltage also increases with capacitance. However, once the capacitance reaches a certain value, the output voltage hardly changes with further increases in capacitance, resulting in a stable efficiency at a certain level. From the graph, it can be observed that when the load current is 1 uA, capacitance values ranging from 60 pF to 200 pF can be considered as optimal,with an efficiency of 47.91% to 49.11%. To make a better comparison with the Dickson charge pump, a capacitance value of 60 pF is chosen.

The selection of output capacitance C_L follows the same considerations as in the Dickson charge pump, taking into account factors such as ripple and frequency. The relationship among the three factors is illustrated in Figure 3.21. Due to the chosen frequency of 100 kHz, in order to maintain a ripple of 25 mV, the chosen value for the output capacitance is 200 pF.

4.2.2.6 Frequency choice

Frequency mainly influences the buffer power consumption,and output voltage. As depicted in Figure 4.22, frequencies ranging from 66.67 kHz to 100 kHz can be considered as the optimal frequency for

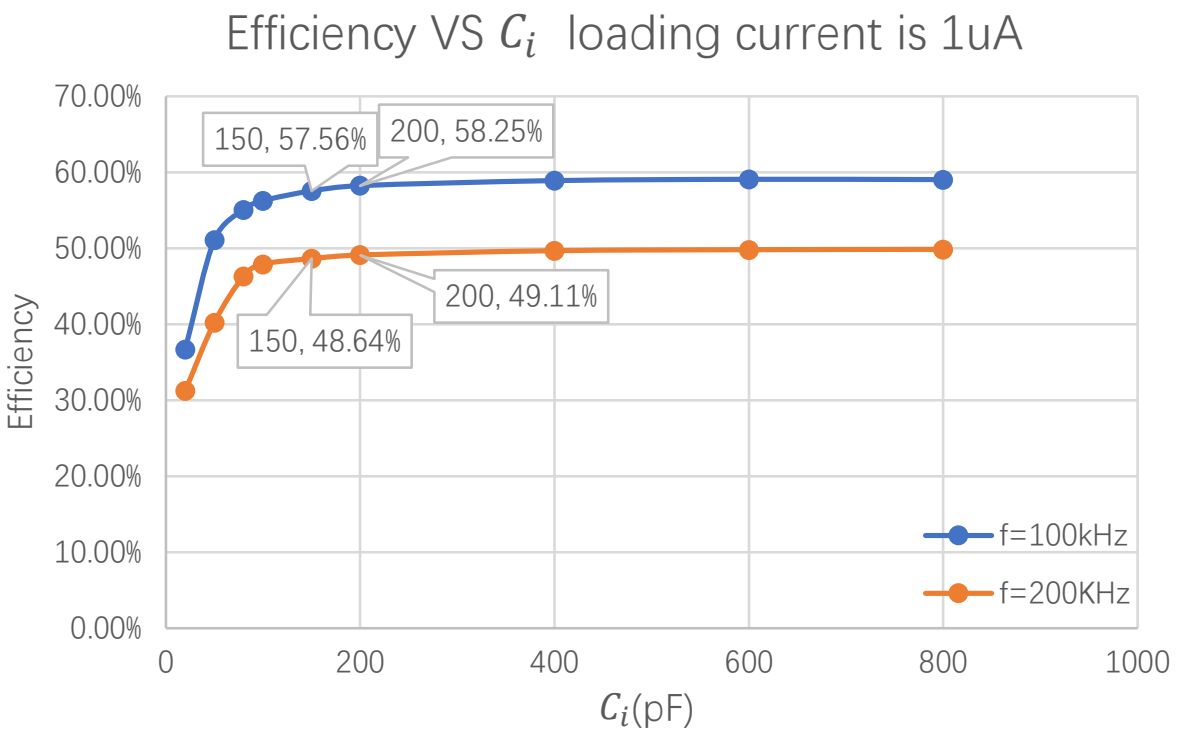


Figure 4.21: Efficiency VS C_i with two frequencies

this topology,with an efficiency of approximately 53%. And small ripple is preferred, so 100 kHz is chosen.

4.2.2.7 Power efficiency optimization

As analyzed in Section 3.6, power efficiency can be expressed as :

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{out} \cdot I_o}{V_{DD} \cdot I_{in} + N \cdot V_{clk} \cdot I_o + C_b \cdot f \cdot V_{clk}^2} \tag{4.13}$$

With increasing the loading current while change the frequency to keep ripple constant, V_{out} will decrease as I_o increases, shown in Figure 4.23, because of the MOSFET size limitations on load current.

With increasing the loading current while change the ripple, there will an optimal loading current as analyzed in section 3.6. In dynamic CTS's topology, efficiency VS loading current is depicted in Figure 4.24.

Figure 4.24 indicates the power efficiency of the circuit when different loading current is added. In this situation, the C_i is 800 pF to reach the maximum efficiency. And frequency is fixed at 100 kHz. Although the ripple will change, the difference is very small. From the graph, it can be observed that the maximum efficiency can reach 67% when the load is 3 uA, whereas the efficiency drops to only 35% when the load is 15 uA.

4.2.3 PMOS NW connection consideration

In the charge pump utilizing dynamic CTS's, the introduction of an inverter utilizes PMOS. Similar to NMOS, PMOS also faces the issue of breakdown voltage. Figure 4.25 represents the layout diagram of PMOS, where bulk, source, and N-WELL are connected together and connected to the high voltage V_i at the output. When V_i exceeds the breakdown voltage, the diode between the N-WELL and the p-substrate becomes reverse biased, leading to PMOS breakdown.

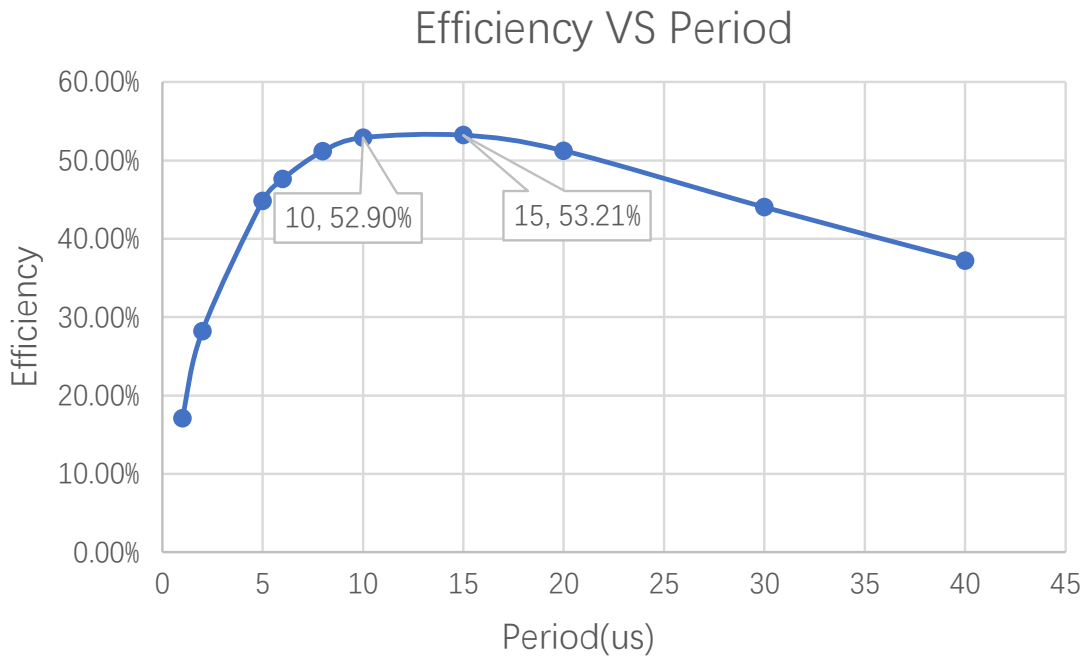


Figure 4.22: Efficiency VS T

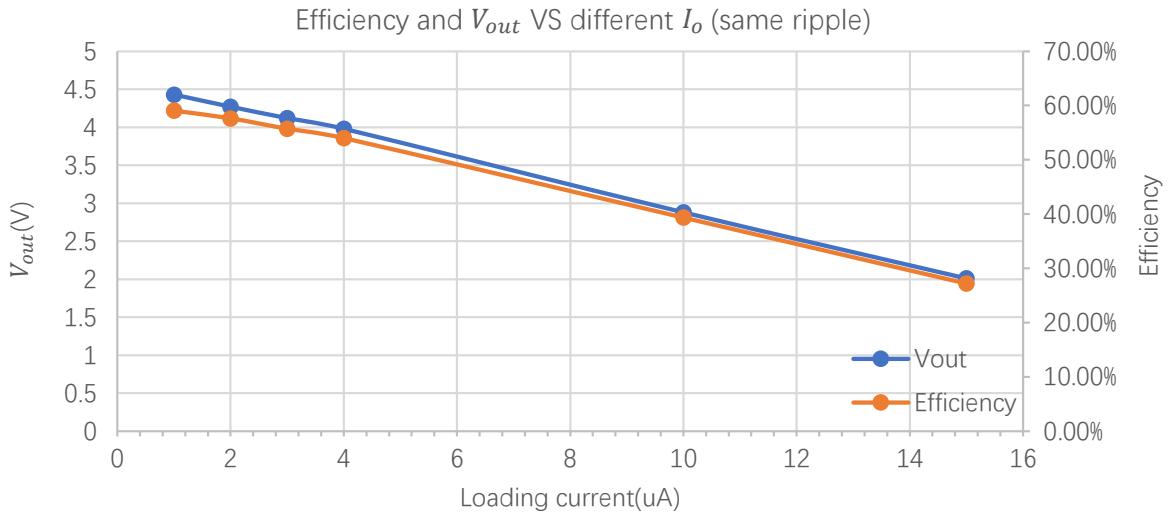


Figure 4.23: Efficiency and V_{out} VS I_0 with same ripple

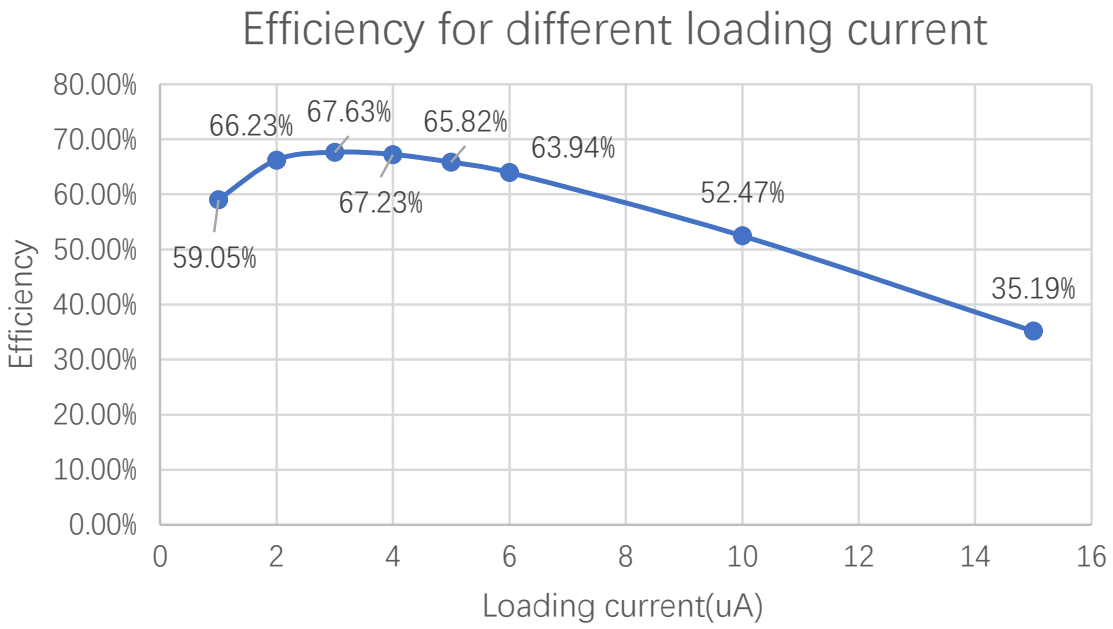


Figure 4.24: Efficiency VS I_0

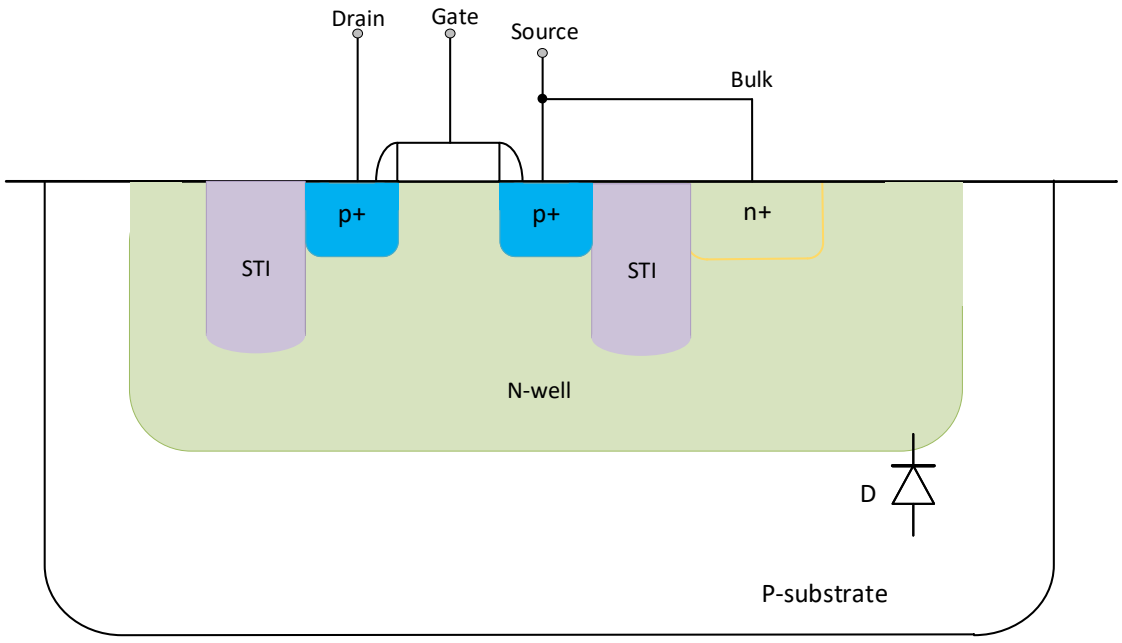


Figure 4.25: Layout of PMOS

4.2.4 Comparison of Dickson charge pump and dynamic CTS's charge pump

Parameters designed in dynamic CTS's is shown in Table 4.1. To analyze four-stage charge pump of

Parameters	Dynamic CTS's
I_o	1 uA
W / L of MOSFET diode	20 um/ 8 um
W / L of MOSFET switch	2 um/ 6 um
W/L of NMOS(inverter)	8 um/ 200 nm
W/L of PMOS(inverter)	1.335 um/ 8 um
Ripple	25 mV
Frequency	100 kHz
C_i	100 pF
C_L	200 pF
Stages	4
V_{out}	4.53 V
Area	0.107 mm^2
Efficiency	60.47%

Table 4.1: Parameters in Dynamic CTS's

two different topologies, given a ripple of 25 mV, for the two topology structures, the optimal values for each parameter are shown in Table 4.2. The situations where C_i equals to 800 pF is to make the circuits get the maximum efficiency, so the area for these two situations does not have much meanings. It can be concluded that for the same topology, parameters that reaches a higher efficiency will cause larger area. And when two topologies has the same parameters, dynamic CTS's has a higher power efficiency occupying same area.

	Stages	Ripple	V_{out}	C_i	Frequency	$C_{L,opt}$	I_o	Efficiency	Area
Dickson	4	25mV	3.25V	800pF	200kHz	100pF	2uA	56.07%	0.589 mm^2
Dickson	4	25mV	3.26V	100pF	100kHz	200pF	1uA	56.41%	0.107 mm^2
Dickson	4	25mV	3.43V	60pF	200kHz	100pF	1uA	53.72%	0.061 mm^2
Dynamic CTS's	4	25mV	4.43V	800pF	100KHz	200pF	3uA	67.63%	0.607 mm^2
Dynamic CTS's	4	25mV	4.53V	100pF	100kHz	200pF	1uA	60.47%	0.107 mm^2
Dynamic CTS's	4	25mV	4.47V	60pF	200kHz	100pF	1uA	43.4%	0.061 mm^2

Table 4.2: Comparison of 4-stage Dickson and Dynamic CTS's

Then extend the stages to get the desired output voltage of 20 V. Table 4.3 and Figure 4.26 depict a comparison of three scenarios. One scenario is when the parameters of the Dickson and dynamic CTS's are set the same, while the other scenario is when the Dickson and dynamic CTS's are set to their respective optimal parameters. The load current is fixed at 1 uA.

	Stages	V_{out}	C_i	C_L	Ripple	Frequency	$T_{settling}$	Area	Efficiency
Dickson	41	20.18V	60pF	100pF	25mV	200KHz	10.34ms	0.457 mm^2	43.33%
Dynamic CTS's	25	20.57V	100pF	200pF	25mV	100KHz	9.45ms	0.482 mm^2	71.15%
Dynamic CTS's	25	20.38V	60pF	100pF	25mV	200KHz	4.48ms	0.285 mm^2	53%

Table 4.3: Comparison of 20V in Dickson and Dynamic CTS's

When all the parameters in Dickson charge pump and dynamic CTS's are same, the dynamic CTS's structure can use a smaller size of $0.285mm^2$ and provide a high power efficiency of 53% to reach the same output voltage of 20V. Also has a lower settling time of 4.48 ms to achieve 95% of 20V. For the

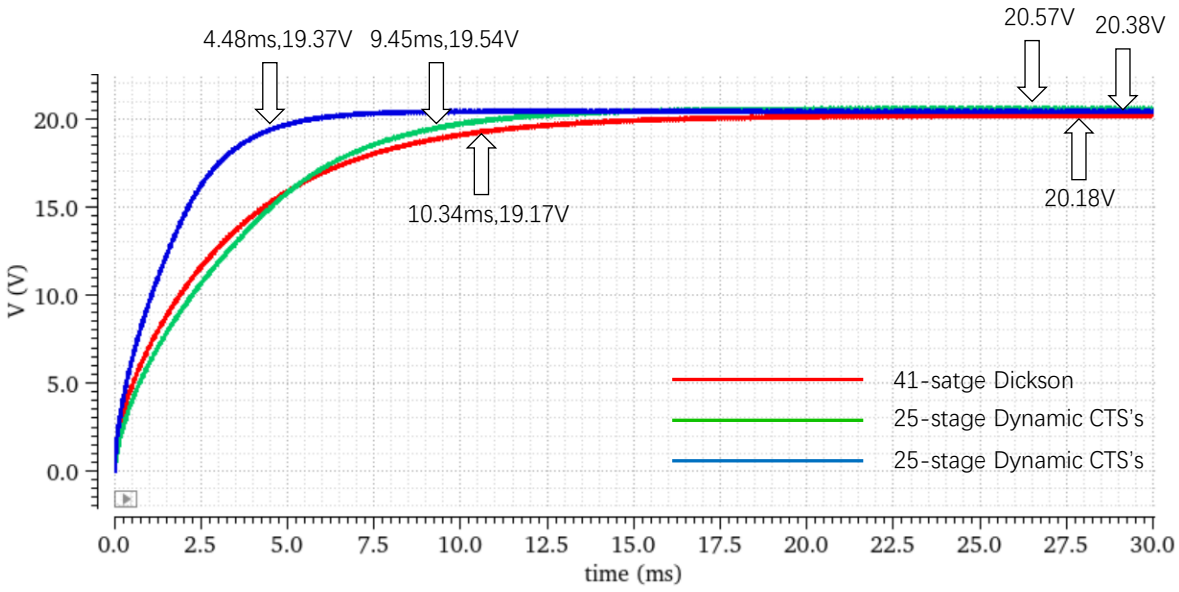


Figure 4.26: Comparison of three situations

respective optimal situation, although higher capacitance and lower frequency can increase the efficiency, more area is occupied. So design which kind of charge pump is a trade-off between the area and power efficiency.

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5

Conclusion

In this thesis, how to generate on-chip high voltage on CMOS device is designed. The objective of this article is to achieve a 20V output using charge pump from a 1.8V supply voltage while simultaneously reducing chip area and improving power efficiency.

Firstly the principle of charge pump is discussed. Charge pumps, irrespective of their structures, essentially exploit the energy storage feature of capacitors and the periodic variation of clock signals to achieve the incremental transfer of charges. The classical Dickson charge pump has been primarily investigated. The detailed analysis encompasses the specific process of charge transfer, along with various parameters such as output voltage, number of stages, settling time, ripple, and power consumption. Furthermore, research has been dedicated to addressing the MOSFET breakdown issue. This involves the utilization of an intermediate voltage for voltage division to halve the voltage across the diodes.

A specific design for the Dickson charge pump was carried out in the next step. Transistor sizes were determined taking into account leakage current and parasitic capacitance. Capacitor and frequency values were designed considering multiple aspects such as output voltage, chip area, power consumption, and ripple. Ultimately, an NMOS transistor with a width of 40 um and a length of 6 um was selected. The value of C_i was chosen as 60 pF, the output capacitance was set to 100 pF, and the frequency was set at 200 kHz.

Under the aforementioned parameters, the four-stage Dickson charge pump is capable of driving a maximum current of 4 uA. However, the efficiency noticeably decreases when the load reaches 5 uA.

The output voltage of the Dickson charge pump is constrained by the threshold voltage. To achieve the desired voltage, more stages are required, resulting in increased chip area and higher power consumption. To address this issue, the utilization of charge transfer switches (CTS's) in charge pumps was investigated to mitigate the impact of threshold voltage loss. Initially, the structure employing static charge transfer switches was explored. However, in the static CTS structure, MOSFETs cannot be fully turned off at specific times, resulting in reverse charge sharing. To address this issue, the investigation extended to dynamic charge transfer switches. In this approach, an inverter was introduced, where the next-stage voltage controlled the behavior of the inverter, thereby governing the opening and closing of the MOSFET switches.

However, the introduction of the inverter introduces the possibility of PMOS breakdown. This occurs because the high voltage of the final stage is directly connected to the PMOS, resulting in the maximum voltage between the PMOS's N-well and p-substrate being V_{out}. If V_{out} exceeds the breakdown voltage (V_{bd}), the PMOS may experience breakdown.

During the design process of the dynamic CTS's, the considerations for the MOSFETs acting as diodes and switches are similar to those of the Dickson charge pump, namely leakage current and parasitic capacitance. The transistor sizes for the diodes were chosen as 20 um for width and 8 um for length, while for the switches, the sizes were selected as 2 um for width and 6 um for length.

However, in the design of the inverter, it is necessary to ensure that the driving capability of the NMOS transistor is sufficiently strong to minimize the time for reverse charge sharing. The final selected sizes for the NMOS and PMOS transistors in the inverter are 8 um/200 nm and 1.335 um/8 um, respectively.The selection of capacitor and frequency values also depended on considerations of chip area and power

efficiency. The optimal capacitance for C_i is 100 pF, C_L is 200 pF and frequency is 100 kHz at a given ripple of 25 mV.

When aiming for a stable output of 20V with a load current of 1 uA, a comparison was made between the Dickson charge pump and the dynamic CTS's circuit structures. The Dickson charge pump requires 41 stages and results in a total chip area of $0.457mm^2$, with an efficiency of 43.33%. In contrast, under the same parameters, the dynamic CTS's only requires 25 stages, resulting in a chip area of $0.285mm^2$ and an efficiency of 53%. And if optimal values of components is designed in dynamic CTS's topology, 25 stages is needed to get a 20V output voltage, with a maximum efficiency of 71.15% and an area of $0.482mm^2$.

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