FACULTY OF ENGINEERING AND ARCHITECTURE

Efficient Sigma-Delta modulators for ultra-deep sub-micron CMOS

Brendan Saux
Student number: 01505795

Supervisor: Prof. dr. ir. Pieter Rombouts
Counsellor: Dr. ir. Johan Raman

Master's dissertation submitted in order to obtain the academic degree of
Master of Science in Electrical Engineering - main subject Electronic Circuits and Systems

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Brendan Saux, May 2020

Preface

This dissertation is the result of a challenging but fulfilling year and I have many people to thank. This thesis could not have been written without the kind help and patience of my supervisor prof. Pieter Rombouts and my counsellor ir. Johan Raman. I'd also like to extend my gratitude to the other members of the CAS team, ir. Jonas Borgmans and ir. Robbe Riem. Also to my friends and family, who have supported me along the way.

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by

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Abstract The increasing miniaturization of transistors over the past half century allowed small and cheap electronic devices to flood consumer markets. While many functions are now performed digitally, the communication systems of these devices remain firmly in the analog domain. Essential to these is the analog-to-digital converter, which is often integrated along digital electronics to minimize costs. However, the low gains and supply voltages in this environment make analog design challenging. One class of power-efficient and robust analog-to-digital converters is the sigma-delta modulator. D. Vercaemer proposed a new digital-to-analog converter for use in the feedback path of continuous-time sigma-delta modulators [1][2]. This would have as main advantages reduced requirements and power consumption for the operational amplifiers. In this dissertation, a sigma-delta modulator is designed using this new digital-to-analog converter. An analysis of the converter is performed and a procedure to extract the system coefficients is developed. The modulator is implemented in the TSMC 65nm low power technology node. It operates at a clock frequency of 2 GHz with an oversampling rate of 48, resulting in a bandwidth of 20.83 MHz. A SDNR of 79 dB and an SNR of 82 dB were obtained.

Keywords sigma-delta modulator, analog-to-digital converter, filtering digital-to-analog converter.

Efficient Sigma-Delta modulators for ultra-deep sub-micron CMOS

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***Abstract*—In this dissertation, a continuous-time third-order sigma delta modulator was implemented using a novel digital-to-analog converter in the feedback path. The resulting circuit provides reduced constraints and a reduced power consumption of the first operational amplifier. The modulator was implemented in the TSMC 65nm low power technology node. The modulator operates at a clock frequency of $2\ GHz$ with an oversampling rate of 48, resulting in a bandwidth of $20.83\ MHz$. A SDNR of $79\ dB$ and an SNR of $82\ dB$ were obtained.**

***Index Terms*—sigma-delta modulator, analog-to-digital converter, filtering digital-to-analog converter.**

I. Introduction

The increasing miniaturization of transistors over the past half century allowed small and cheap electronic devices to flood consumer markets. While many functions are now performed digitally, the communication systems of these devices remain firmly in the analog domain. Essential to these is the analog-to-digital converter, which is often integrated along digital electronics to minimize costs. However, the low gains and supply voltages in this environment make analog design challenging. One class of power-efficient and robust analog-to-digital converters is the sigma-delta modulator. D. Vercaemer proposed a new digital-to-analog converter (DAC) for use in the feedback path of continuous-time sigma-delta modulators [1][2]. In this dissertation, a sigma-delta modulator is designed using this new DAC.

II. Low-pass filtering switched-capacitor DAC (LPSC DAC)

A. Motivation

Due to thermal noise constraints on the resistors, the current consumption in a sigma-delta modulator will be dominated by the first integrator. This current consumption is proportional to ϵ, the difference between the input signal $X(s)$ and the feedback signal V_{fb}. For low frequencies, the negative feedback will cause V_{fb} to be approximately equal to $X(s)$, resulting in a very small ϵ. Most of the current consumption of the first integrator will thus be caused by high-frequency out-of-band quantization noise. Filtering in the feedback path can filter out this high-frequency noise and therefore strongly reduce this current consumption. This filtering operation is usually performed in continuous time after the DAC, which does not reduce errors such as clock jitter at the DAC, since these have already entered the system. A more robust alternative is filtering in discrete-time within the DAC itself. These errors are then filtered out before they can influence the system.

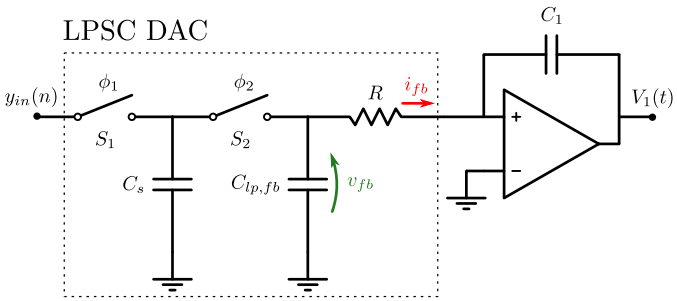

Fig. 1. LPSC DAC.

B. Analysis

The circuit proposed to perform this filtering is shown on figure 1 [1][2]. A sampling capacitor C_s is placed between two switches driven by non-overlapping clock phases ϕ_1 and ϕ_2, shown on figure 3. When ϕ_1 is high, C_s is charged to $V_{ref+} = 1.2\ V$ or discharged towards $V_{ref-} = 0\ V$, depending on the output bit $y(n)$. The input voltage can thus be expressed as $y_{in}(n) = V_{ref+}y(n)$. When ϕ_2 goes high, C_s and $C_{lp,fb}$ are placed in parallel and their charge is redistributed. After switching, this voltage will experience an exponential decay through the resistor R. This decay can be approximated by a decay with a time constant $\tau = RC_{lp,fb}$. The total decay over a clock period is called γ

$$\gamma = e^{-\frac{T_s}{\tau}} \tag{1}$$

Taking into account this exponential decay and calling $\beta = \frac{C_s}{C_{lp,fb}+C_s}$, the z-transform of the transfer function $H_{lp}(z)$ from the input $Y_{in}(z)$ to $V_{fb}(z)$ is

$$H_{lp}(z) = \frac{V_{fb}(z)}{Y_{in}(z)} = \frac{\beta}{1-(1-\beta)\gamma z^{-1}} \tag{2}$$

The Laplace transform of the exponential decay through the resistor is

$$P(s) = \frac{1-\gamma e^{-sTs}}{s\tau+1}\frac{\tau e^{-sT_1}}{R} \tag{3}$$

The total transfer function of the LPSC DAC is the product of the discrete-time low-pass filter $H_{lp}(z)$ and the exponential decay $P(s)$

$$H_{DAC}(s) = P(s)H_{lp}(z)|_{z=e^{sT_s}} \tag{4}$$

The impulse response corresponding to this transfer function is plotted on figure 4.

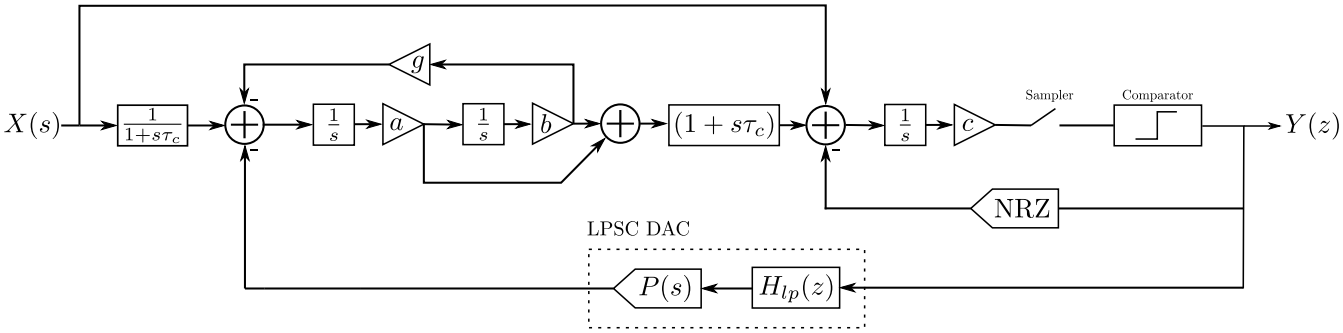

Fig. 2. Total system.

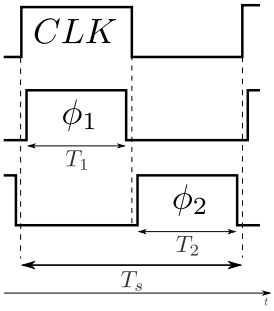

Fig. 3. Clock phases of the LPSC DAC.

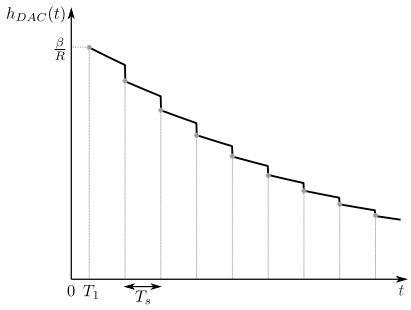

Fig. 4. Impulse response of the LPSC DAC.

III. Compensating the DAC

The LPSC DAC impulse response consists of a digital low-pass filter and a delayed exponentially decaying pulse, which will increase the order of the modulator by 1. Ideally, the noise transfer function design should be independent of the LPSC DAC. This can be accomplished by compensating the introduced pole by adding a compensating zero τ_c to the continuous-time loop filter. This changes the signal transfer function as well, which is restored by adding a pole τ_c to the input branch. The proposed changes are indicated in red on figure 5.

IV. System Design

The proposed design is shown on figure 2 and based on [7]. It is a third-order sigma-delta modulator using a cascade of integrators with feedforward and feedback. The feedforward

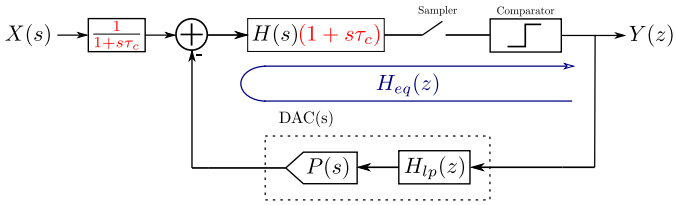

Fig. 5. Compensating the LPSC DAC.

path leads to a smaller internal signal swing at the first integrator and better noise suppression. The outer feedback loop uses the LPSC DAC and the inner path makes use of a non-return-to-zero (NRZ) DAC. A local feedback path with gain g is introduced, which allows the zeros of the noise transfer function to be optimized. Placing the zeros of the noise transfer function close to the signal bandwidth will minimize the in-band noise [8]. An input feed-in in front of the last integrator relaxes the requirements on the second integrator by providing the necessary low-frequency content to compensate the DAC signal of the inner loop.

The NTF of the modulator is obtained using the Delta Sigma Toolbox designed by R. Schreier [6], choosing a maximum out-of band gain $||H_\infty|| = 1.5$ for stability, following M.L. Lee [5]. Based on this NTF, a desired equivalent discrete-time loop filter $H_{eq,des}$ is found

$$\begin{aligned} H_{eq,des}(z) &= \frac{1}{NTF} - 1 \\ &= 0.79851\frac{(z^2 - 1.641z + 0.6964)}{(z-1)(z^2 - 1.998z + 1)} \end{aligned} \tag{5}$$

The actual equivalent discrete-time loop filter $H_{eq}(z)$ is found by summing all the paths around the loop of the system and is

$$\begin{aligned} H_{eq}(z) = \Big[(s\frac{ac\tau_c}{(s^2+\omega_z^2)} + \frac{ac + abc\tau_c}{(s^2+\omega_z^2)} \\ + \frac{abc}{s(s^2+\omega_z^2)})P(s)\Big]^* H_{lp}(z) + \frac{c}{z-1} \end{aligned} \tag{6}$$

Where $\omega_z^2 = gab$ is caused by the local feedback. The * represents the effect of the sampling operation and is called the star operator, which is described in works as [4]. Equations

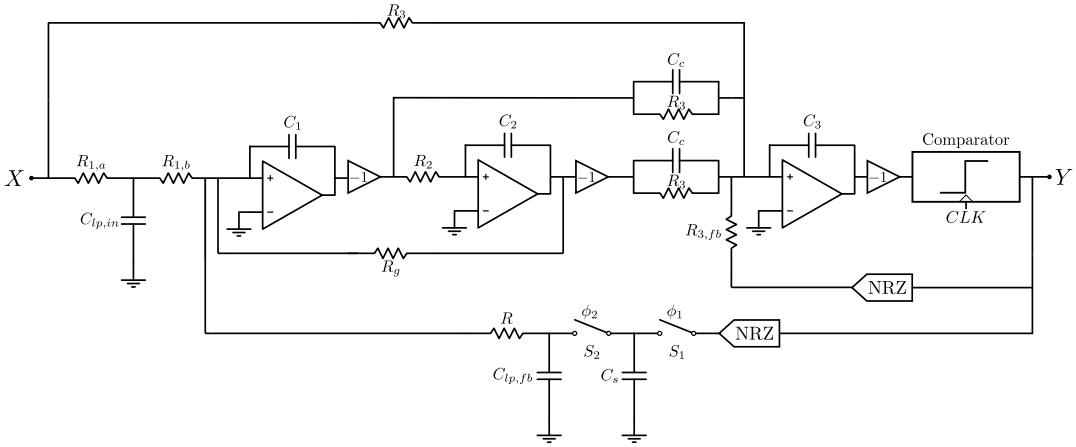

Fig. 6. Circuit overview.

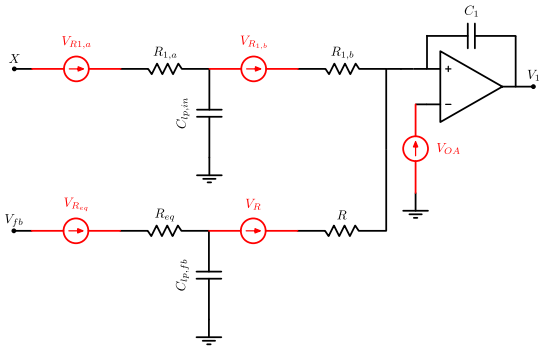

Fig. 7. Low-frequency approximation of the input and feedback branch of the modulator.

(5) and (6) can be equated to find the unknown coefficients a, b, c and the compensating zero τ_c.

V. Circuit

The system of figure is now implemented differentially with RC-active integrators. It is shown on figure 6. The compensating zero is obtained by a capacitor C_c in parallel with the third resistor R_3. The pole in the input branch was implemented as a capacitor $C_{lp,in}$ to ground between $R_{1,a}$ and $R_{1,b}$.

A. Sizing τ

τ will be sized based on limitations of the input-referred thermal noise in the input and feedback branches. It is first observed that at low frequencies, the switched capacitor circuit around C_s can be approximated as an equivalent resistor R_{eq}. The input and feedback branches can then be approximated as on figure 7, with the thermal noise sources due to the resistors and opamp indicated in red. In order to have an STF as close as possible to 1, the sum of R_{eq} and R must satisfy

$$R + R_{eq} = R_1 = R_{1,a} + R_{1,b} \tag{7}$$

The input-referred power of the resistors can now be found by superposition as

$$P_{in,R} = 16 k_B T f_b R_1 \left(1 + \frac{(2\pi f_b \tau_c)^2}{3}\left[\frac{R_1}{2R_{1,b}} + \frac{R_1}{2R}\right]\right) \tag{8}$$

The input-referred power of the opamp is found similarly

$$P_{in,OA} = \gamma\alpha \frac{k_B T f_b}{g_m}\left(1 + \frac{(2\pi f_b \tau_c)^2}{3}\left[\frac{R_1}{2R_{1,b}} + \frac{R_1}{2R}\right]^2\right) \tag{9}$$

Where γ represents how deep the MOSFET channels are inverted and α represents the effective amount of transistors that contribute to the thermal noise. g_m is chosen to result in an equal thermal noise contribution of the opamp as the resistors. It will be demanded that the noise increase due to the low-pass filtering stay be no more than $1\ dB$. This leads to $\tau_c = \frac{1}{5\pi f_b}$ and

$$\tau = \frac{2}{5\pi f_b} \tag{10}$$

B. Resistor sizing

Reducing thermal noise in sigma-delta modulators can only be accomplished by impedance scaling, which leads to a large increase in power consumption. Reducing quantization noise is more power-efficient and can be performed by using a more aggressive noise transfer function or adding an integrator, which takes up only a limited amount of extra power. Therefore, a rule of thumb is placing the thermal noise $10 - 12\ dB$ higher than the quantization noise [3]. For an input signal of $-6\ dBFS$, an SNR of $82\ dB$ is obtained, which means the quantization noise floor is at $88\ dBFS$. Following the previously mentioned rule of thumb, the thermal noise will be placed $12\ dB$ higher at $76\ dB$. To determine the resistor sizing, three noise sources N_1 to N_3 are added to the system as shown on figure 8. These represent the thermal noises at the inputs of each integrator. The transfer functions of each noise source to the output are given by

$$H_1(f) = \frac{V_{out}}{N_1} = NTF(z)\left[\frac{(as + ab)(1 + s\tau_c)}{s^2 + \omega^2}\frac{c}{s}\right] \tag{11}$$

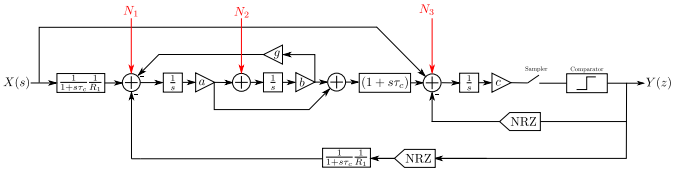

Fig. 8. System with added noise sources.

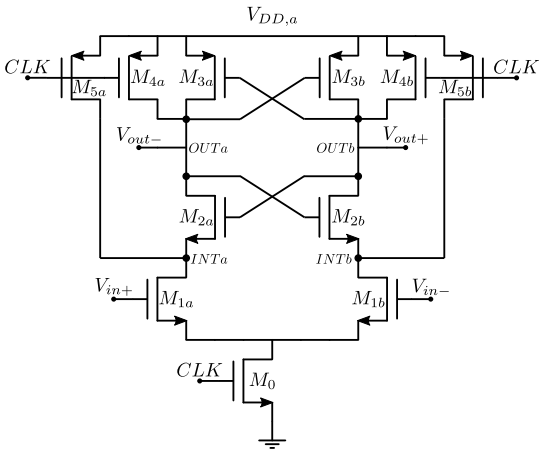

Fig. 9. StrongARM comparator.

$$H_2(f) = \frac{V_{out}}{N_2} = NTF(z)\left[\frac{(bs-\omega^2)(1+s\tau_c)}{s^2+\omega^2}\frac{c}{s}\right] \quad (12)$$

$$H_3(f) = \frac{V_{out}}{N_3} = NTF(z)\left[\frac{c}{s}\right] \quad (13)$$

The contribution of N_1 will be almost unsuppressed in comparison to N_2 or N_3. The highest noise budget is therefore allocated to N_1. The resistor values are then obtained by demanding the noise power of each noise source referred to the output lie below the allocated budget. The noise power of the k'th noise source N_k at the output is

$$P_k = \int_0^{f_b} |H_k(f)|^2 S(f) df \quad (14)$$

Where f_b is the signal bandwidth and $S(f)$ the noise spectral density of the noise source.

C. Comparator

The used comparator is the classic StrongArm latch. It is displayed on figure 9. It is a compact comparator, boasting rail-to-rail outputs and zero static power consumption. It consists of a differential pair with two cross-coupled invertors [9]. Its operation is based on 4 phases. When the clock signal CLK is low, the internal nodes are precharged to the analog supply voltage $V_{DD,a}$. When CLK goes high, a common mode-current will flow while the differential input voltage is amplified on the node INT. This continues until the cross-coupled NMOS pair turns on. The amplification now continues on the OUT node, reinforced by the charge transfer from INT to OUT by the cross-coupled NMOS transistors. Finally, the

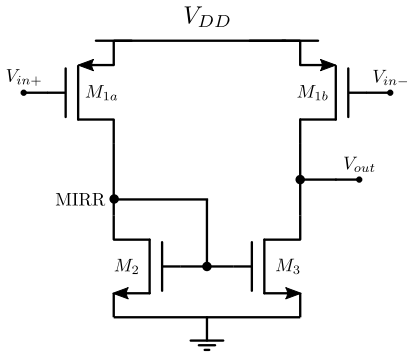

Fig. 10. Set-reset stage.

PMOS transistors turn on and the differential output voltage exponentially regenerates. The entire cycle repeats when CLK goes low [10][11].
The transistors M_2 and M_3 are equally sized to reduce parasitic capacitance and obtain the same transconductance. It is beneficial to increase them in size until their parasitic capacitance dominates the load capacitance. The input differential pair M_1 and tail transistor M_0 are sized to obtain a large current of 300 μA through each of the differential pair transistors.

D. set-reset stage

To maintain the output of the comparator during the reset phase, the comparator is followed by a set-reset stage, inspired by . Shown on figure 10, it consists of two input PMOSFETS and and a current mirror. When is high, will be pulled high. When V_{in+} is high, the internal node $mirr$ is pulled high and V_{out} is pulled low. The NMOS M_2 is sized minimally to reduce current consumption. The PMOS transistors M_{1a} and M_{2a} are sized three times larger, to take into account different carrier mobility. The current mirror introduces a delay in the propagation delay from V_{in+} to V_{out} compared to the propagation delay from V_{in+} to V_{out}. To minimize this propagation time, M_3 is sized 3 times larger than M_2.

E. Metastability

Though the comparator seemed to behave as designed in initial simulations, a large SNR degradation was observed when it was integrated in the sigma-delta modulator. The cause of the problem was narrowed down to the inner loop, since the effect of the local feedback in the outer loop was still visible in the modulator output spectrum. After other possible causes were excluded, it was decided to investigate the effects of various non-idealities of the real comparator waveform on the modulator. To this end, an ideal verilogA comparator was used and modified to include each of the studied non-idealities. Finally, the cause of the SNR was found as the metastability of the comparator, in which the regeneration time for small signals is severely increased. This signal-dependent delay leads to a variable feedback, which reduces the SNR. As long as C_s is charged before ϕ_2, the LPSC DAC is not

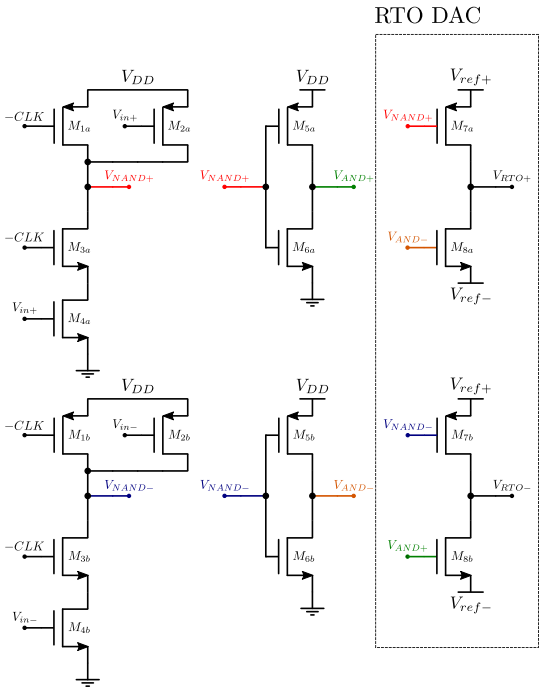

Fig. 11. Circuit to generate RTO pulse.

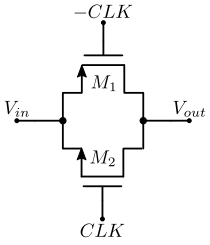

Fig. 12. Transmission gate S_2.

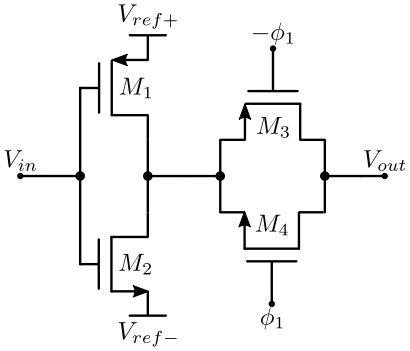

Fig. 13. DAC and transmission gate S_1.

influenced by the comparator metastability. The problem is the NRZ DAC in the inner loop. This DAC is modified in a DAC with a fixed half clock cycle delay that provides a pulse lasting half a clock cycle. At the time instants where there is no feedback pulse, the DAC transistors are in cutoff. This is a return-to-open (RTO) DAC. The fixed delay guarantees a stable comparator output when the RTO pulse is generated. The circuit to implement this is shown on figure 11. Two NAND gates followed by two invertors generate the internal signals of the RTO DAC. During the later half of the clock period, $-CLK$ is high and the output V_{RTO+} switches to V_{ref+} if the bit V_{D-} is high and V_{ref-} if V_{D+} is low. The opposite is true for V_{RTO-}. To maintain the feedback current through the DAC in the inner path, the resistance $R_{3,fb}$ was halved to 25 $k\Omega$.

F. RTO DAC

The RTO DAC is shown on the right of figure 11 and consists of a PMOS switch to $V_{ref+} = 1.2\ V$ and an NMOS switch to $V_{ref-} = 0\ V$. It operates in triode, so will introduce a resistance that must be taken into account by reducing $R_{3,fb}$.

G. LPSC DAC

1) Switch S_2: S_2 on figure 12 will be the switch through which the charge transfer between C_s and $C_{lp,fb}$ takes place. To conduct for a full range of input values, a transmission gate is used, consisting of an NMOS and PMOS transistor in parallel clocked with opposite clock signals ϕ_2 and $-\phi_2$. The switch resistance will be a nonlinear function of the input voltage, which will cause distortion and cause harmonics to appear. To provide the largest range of linearity, the NMOS resistance for a 0 V input and the PMOS resistance for a 1.2 V input are chosen equal. The effect of the nonlinear resistance can be minimized by increasing the size of the transistors, but this will increase the highly nonlinear junction capacitances. The optimal sizing is obtained via simulation.

2) Switch S_1: To charge C_s, the LPSC DAC switches between V_{ref+} and V_{ref-}, but should only do so during ϕ_1. Therefore, the circuit of figure 13 is used, in which a switch to V_{ref+} and V_{ref-} is followed by a transmission gate switch that is clocked on ϕ_1. Unfortunately, charging C_s leads to a very large power consumption. C_s can either be reduced in size by reducing the resistor R and increasing $C_{lp,fb}$ to obtain the same τ or by relaxing the thermal noise requirements.

3) DAC driver: A tapered buffer is used between the LPSC DAC and the SR stage to drive the LPSC DAC switches within an acceptable timeframe. In a tapered buffer, N invertors are chained and each invertor is sized β times larger than the previous one. The model introduced by [12] is used, in which the output capacitance is split up in inherent output capacitance C_x and a load output capacitance C_y. Each invertor is approximated as an equivalent resistance as is usual in digital circuits. To minimize power consumption but meet timing constraints, $N = 3$ and $\beta = 6.28$ are chosen.

H. Clock generator

A simple non-overlapping clock generator is used, which is displayed on figure 14. The OR gate and inverters introduce a delay that prevents the clock signals ϕ_1 and ϕ_2 to go up before the other has gone down. Since the comparator delay and DAC driver delay lead to a large interval in which C_s was charged to the wrong voltage, the clock phases ϕ_1 and

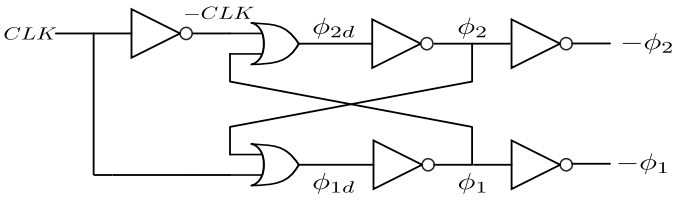

Fig. 14. Clock generator.

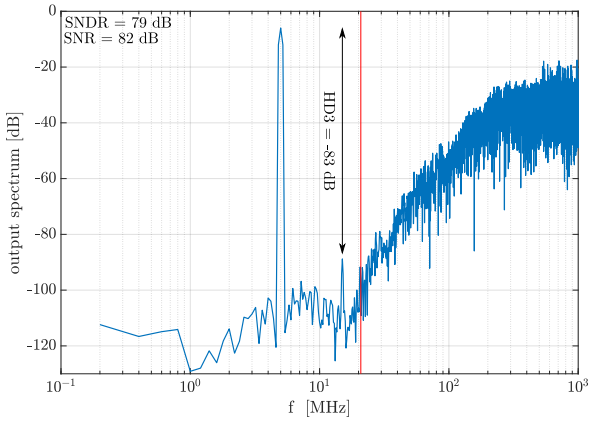

Fig. 15. Output spectrum of the final circuit for a $-6\ dBFS$ input signal of 5 MHz.

ϕ_2 were switched, resulting in an additional half clock cycle delay of the LPSC DAC. This allocated an entire half clock cycle for the comparator to make a decision and this decision to propagate through the tapered buffer of the DAC driver. This lead to C_s only being charged to the correct voltage and reduced power consumption. The additional delay was taken into account by recalculating τ_c and integrator coefficients and modifying the system accordingly.

VI. Results

Finally, the circuit was simulated and compared to a reference system with NRZ DACs. It was clear that the current delivered by the first opamp and its requirements were greatly reduced. The reduced requirements will also lead to a much more efficient design of the opamps. The output spectrum of the final circuit is plotted on figure. A signal to noise and distortion ratio (SNDR) of $SNDR = 79\ dB$ and a signal to noise ratio (SNR) of $SNR = 82\ dB$ are obtained. The third harmonic distortion (HD3) is $-83\ dB$. The SNR conforms to expectations, but the HD3 and SNDR are respectively higher and lower than expected. This discrepancy is probably caused by the non-overlap time of the clock phases being to small. This will cause S_1 and S_2 to overlap when switching on and off.

VII. Conclusion and Future Work

In this dissertation, a continuous-time sigma-delta modulator was developed achieving an SNDR of 79 dB and an SNR of 82 dB. Future work includes designing a transistor level implementation of the clock phase generator, investigating the effect of the non-overlap time of the clock phases on the harmonics and the integration of the operational amplifiers developed in a companion thesis in the sigma-delta modulator.

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Contents

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List of Abbreviations

ADC analog-to-digital converter.

CT continuous-time.

DAC digital-to-analog converter.

dBFS dB relative to full scale.

DT discrete-time.

HD3 third harmonic distortion.

LPSC low-pass filtering switched-capacitor.

NRZ non-return-to-zero.

NTF noise transfer function.

opamp operational amplifier.

RTO return-to-open.

SDM sigma-delta modulator.

SNDR signal to noise and distortion ratio.

SNR signal to noise ratio.

STF signal transfer function.

Chapter 1

Introduction

1.1 Background

The increasing miniaturization of transistors unleashed technological advances that shape our world to this day, allowing small and cheap electronic devices to flood consumer markets. The wireless communication capabilities of many of these devices play an important role in our daily lives, allowing us to stay in contact with coworkers and loved ones, watch videos on the internet and so on. Essential to these capabilities is the analog-to-digital converter (ADC), which is often integrated along digital electronics to minimize costs. This is a hostile environment for analog electronics, as the miniaturization has led to low gains and supply voltages. This introduces new challenges and opportunities, spurring analog designers to develop new techniques to obtain more robust and efficient ADCs. One power-efficient and robust class of ADC is the sigma-delta modulator (SDM), which forms a active research domain.

1.2 Goal

This thesis will continue on the work of D. Vercaemer [1][2]. The main goal for this thesis is developing a sigma-delta modulator with his proposed digital-to-analog converter (DAC) in the feedback path, leading to reduced power consumption and reduced constraints on the operational amplifiers (opamps) as its main advantages. The modulator should have a useful bandwidth of about 20 Mhz and a sample rate of $f_s = 2GHz$. The circuit is implemented in the TSMC 65 nm low power technology.

1.3 Organization

The following chapters are organized as follows. The next chapter will introduce the basic concepts behind analog-to-digital conversion and sigma-delta modulation, paying special attention to continuous-time (CT) sigma delta modulation. In chapter 3 the proposed DAC is analysed and discussed. It can be concluded that the DAC increases the order of the system by 1. In chapter 4, a system-level design is presented, taking into account the added pole and introducing

a compensating zero. The procedure to determine the integrator coefficients and and compensating zero is illustrated. Chapter 5 discusses the circuit-level implementation and design of the main analog building blocks. It will become clear that designing for low supply voltages and high sampling frequencies introduces many challenges that were not predicted during the system-level design, leading to some adjustments. The operational amplifiers are designed in a companion thesis, that is unfinished as of now. The performance of the final circuit is simulated. The thesis ends with some concluding remarks and future work.

Chapter 2

Analog-to-digital conversion

2.1 Introduction

Bridging the gap between analog systems and digital electronics requires ADCs, electronic circuits designed to convert analog signals to digital data. While ADCs exist in many shapes and forms, they invariably perform 2 operations: sampling and quantization. This discussion will mostly be based on [4] and [5].

Sampling

Sampling consists of converting a continuous-time signal to a a discrete-time signal, a series of datapoints containing values of the continuous-time signal at specific time instances, separated by a sampling period T_s. A continuous-time signal can be perfectly reconstructed from a discrete-time signal if it satisfies the *Shannon-Nyquist theorem*. This theorem states that, given a signal with a limited bandwidth f_b and a sampling frequency f_s, no information is lost by sampling the signal if

$$f_s > 2f_b \tag{2.1}$$

$f = 2f_b$ is called the Nyquist frequency. Sampling at a higher frequency than the Nyquist frequency is called oversampling, a concept that will be essential in discussion of SDM operation. The extent to which a signal is oversampled is expressed in the oversampling ratio (OSR)

$$OSR = \frac{f_s}{2f_b} \tag{2.2}$$

The effect of the sampling operation is shown for a sinusoidal input signal on figure 2.1a. The sampled output is represented by black dots. V_{FS} and $-V_{FS}$ are the positive and negative full-scale voltages.

Quantization

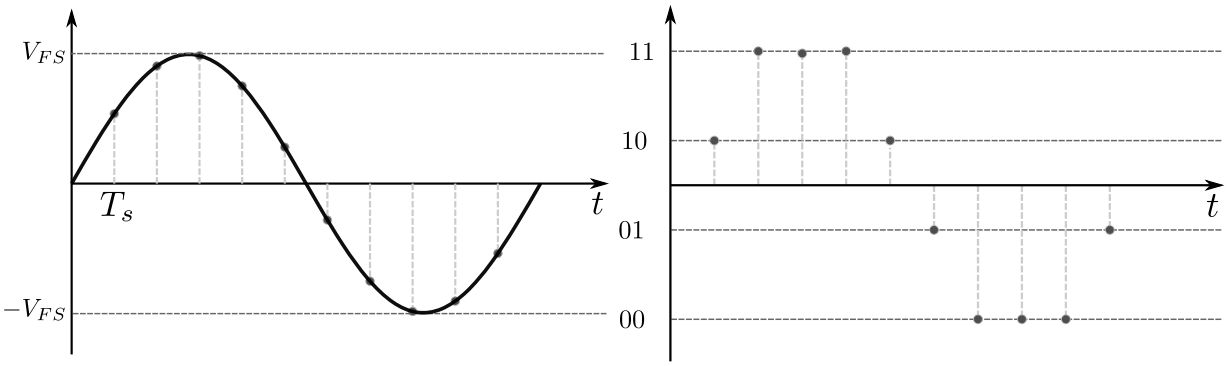
Quantization is the process of converting the values of a signal from continuous range to a limited set of values, the *quantization levels*. The input values are rounded to the nearest quantization

level, allowing them to be represented using a fixed amount of bits.

In a uniform quantizer, all quantization levels are separated by the *quantization step* Δ. With B the number of bits and V_{FS} the full-scale voltage, it can be calculated as:

$$\Delta = \frac{2V_{FS}}{2^B} \tag{2.3}$$

As an example, the sampled signal of 2.1a is further quantized using a two-bit quantizer. The result is shown on 2.1b. The input-output voltage characteristic of a mid-rise quantizer with B-bits is shown on 2.2, along with the the introduced error q on figure 2.3.



(a) Sampling operation.

(b) Two bit quantization of the sampled data.

Figure 2.1: Sampling and quantization of an example sinusoidal waveform with sampling period T_s.

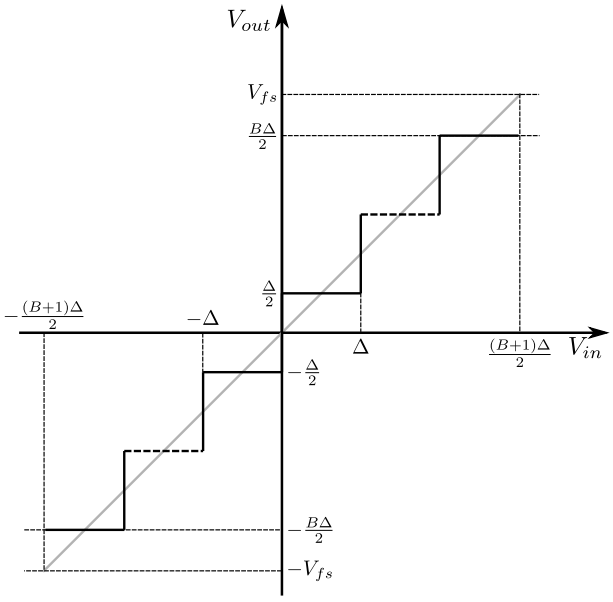


Figure 2.2: Output of a B-bit mid-rise quantizer.

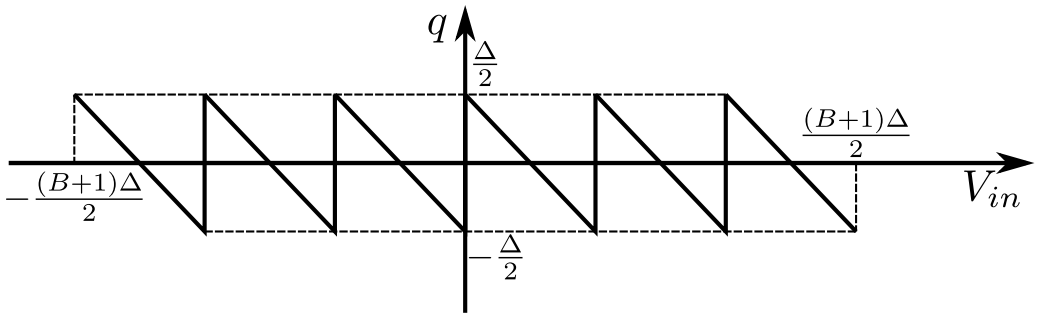


Figure 2.3: errors q of the B-bit mid-rise quantizer.

The errors introduced by the quantizer can be analyzed by approximating the quantizer as an added uniformly distributed noise source. This is an often-used approach when analyzing sigma-delta modulators and this discussion will follow suit. The noise is uniformely distributed between 0 and $f_s/2$ with a total noise power of

$$P_q \approx \frac{2\Delta^2}{12} \tag{2.4}$$

2.2 Sigma-delta modulators

Quantization errors can be reduced by using a large set of quantization levels, but this is not always ideal. Each quantization level usually needs a separate comparator, which leads to large circuit areas and increased costs. Additionally, smaller quantization steps mean the comparators must be increasingly accurate. Another approach in which the limited accuracy of quantizers can be overcome is by placing the quantizer in a feedback loop and oversampling, which leads to the SDM architecture.

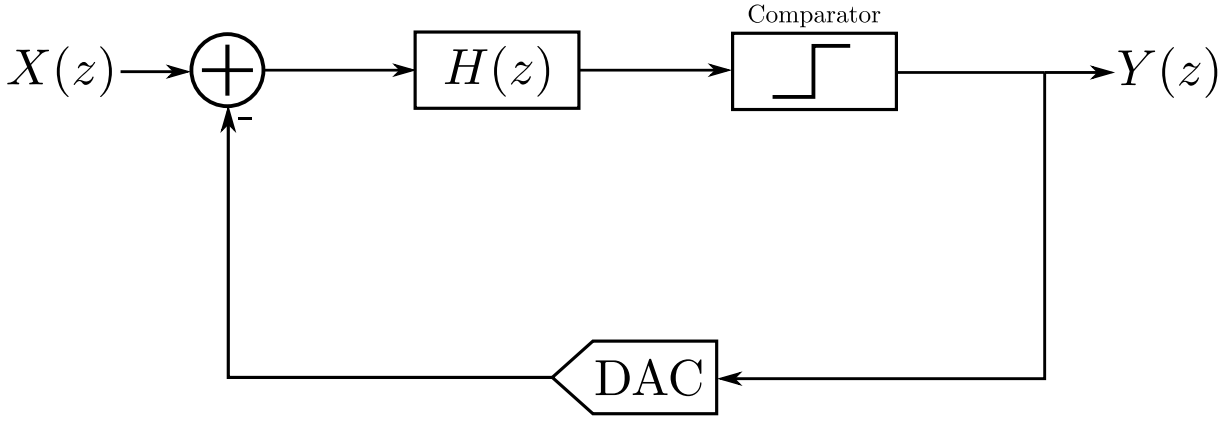


Figure 2.4: DT SDM.

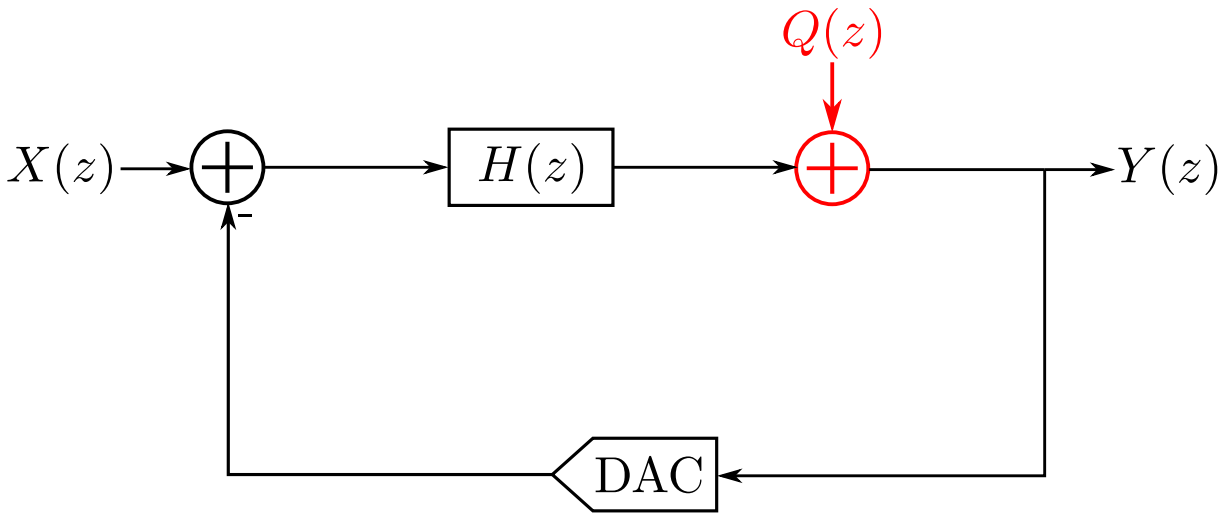


Figure 2.5: DT SDM with uniform noise source approximation of the comparator(red).

A simple example of a discrete-time (DT) SDM design is shown on figure 2.4. The sampling is performed before the modulator. The input and output signal are called $x(n)$ and $y(n)$, with Z-transforms $X(z)$ and $Y(z)$. The input signal $X(z)$ is passed through a filter $H(z)$ and quantized. The output signal $Y(z)$ is fed back and substracted from $Y(z)$, providing negative feedback. The quantizator is approximated as an added white noise source $Q(z)$ on figure 2.5.

2.2.1 Basic Operating principle

SDMs are based on two main principles: oversampling and noise-shaping.

As mentioned in subsection 2.1, the noise spectral density $Q(z)$ after sampling is uniformly distributed between $[0; f_s/2]$ or equivalently $[0; f_b OSR]$. If we increase the sampling frequency f_s, the total noise in the band $[0; f_s/2]$ stays the same, but the noise spectral density will decrease. The total noise in the useful signal band $[0, f_b]$ will consequently also decrease and is simply given by

$$P_q = \frac{2\Delta^2}{12}\frac{1}{OSR} \tag{2.5}$$

The second principle underlying sigma-delta modulation is noise shaping. Because of the presence of the filter $H(z)$ and the feedback path, the output signal of the modulator can found as

$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}Q(z) \tag{2.6}$$

$$= STF(z)X(z) + NTF(z)Q(z) \tag{2.7}$$

Where the signal transfer functions (STFs) and noise transfer functions (NTFs) were defined. $H(z)$ will be designed as a low-pass filter, causing $NTF(z)$ to be a high-pass filter. The noise $Q(z)$ to the output signal is said to be *shaped* by the noise transfer function. Noise is pushed away from the low to higher frequencies. Most of the total noise will therefore fall outside of the

useful bandwidth, where it is easily filtered out. This form of $H(z)$ also leads to $STF(z) \approx 1$ at low frequencies.

The effects of these two principles are summarized on figure 2.6. The sampling frequencies before and after oversampling are denoted F_{s1} and F_{s2} respectively. It is clear that the combination of oversampling and noise-shaping will lead to a strongly reduced noise power in the useful signal bandwidth.

The in-band quantization noise power can be calculated as:

$$P_Q = \frac{1}{2\pi f_s} \int_0^{\omega_b = 2\pi f_b} |NTF(z)|^2 \frac{\Delta^2}{2} d\omega \tag{2.8}$$

This can be calculated for ideal NTFs of order L of the form

$$NTF = (1 - z^{-1})^L \tag{2.9}$$

which ultimately leads to

$$P_Q = \frac{\Delta^2}{12\pi(2L+1)} (\frac{\pi}{OSR})^{2L+1} \tag{2.10}$$

This last equation illustrates the power of noise shaping. For a third-order modulator, which this implemented in this thesis, the noise power decreases with the seventh power of the OSR!

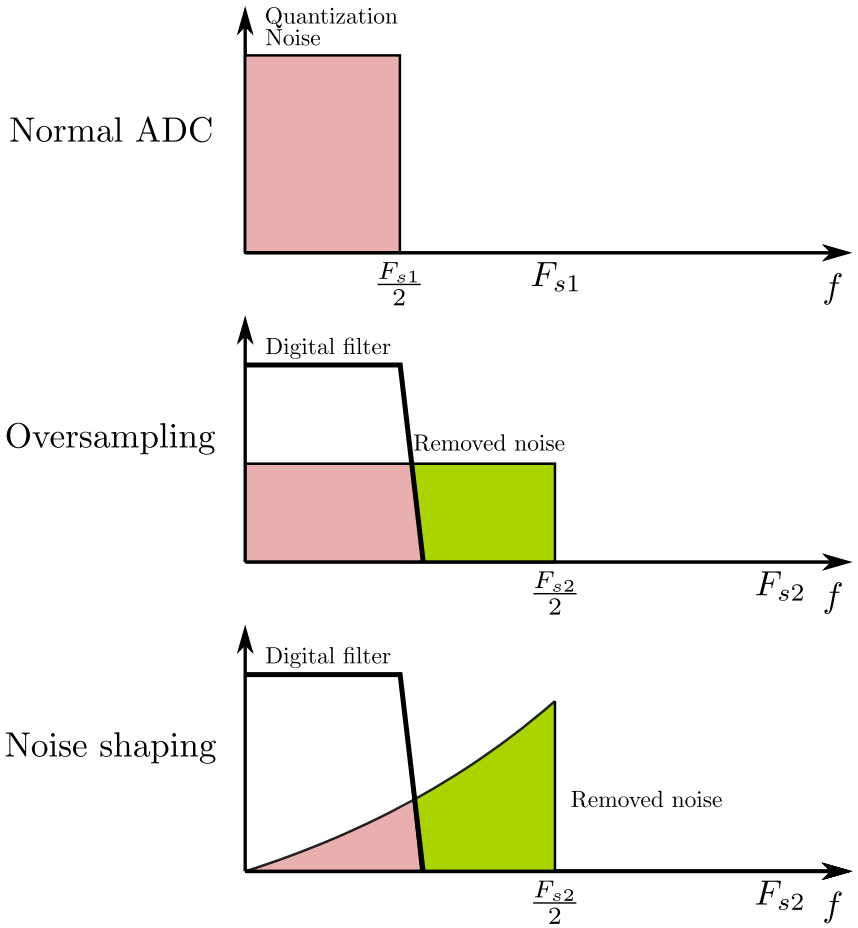


Figure 2.6: Sketch illustrating the effects of oversampling and noise shaping.

2.2.2 Continuous-time sigma-delta modulators

DT SDMs as described in the previous paragraphs offer a lot of advantages. The used switched-capacitor filters are easily realized and the mathematical description is relatively simple. However, a possible alternative is operating the SDM in CT. This will have some important consequences, and will allow us to remove the costly anti-aliasing filter. In the CT SDM, the sampling will be performed inside the feedback loop, instead of in front the loop. Therefore, the loop filter will no longer be DT. This will relax the gain-bandwidth requirements on the opamps in the loop filter.

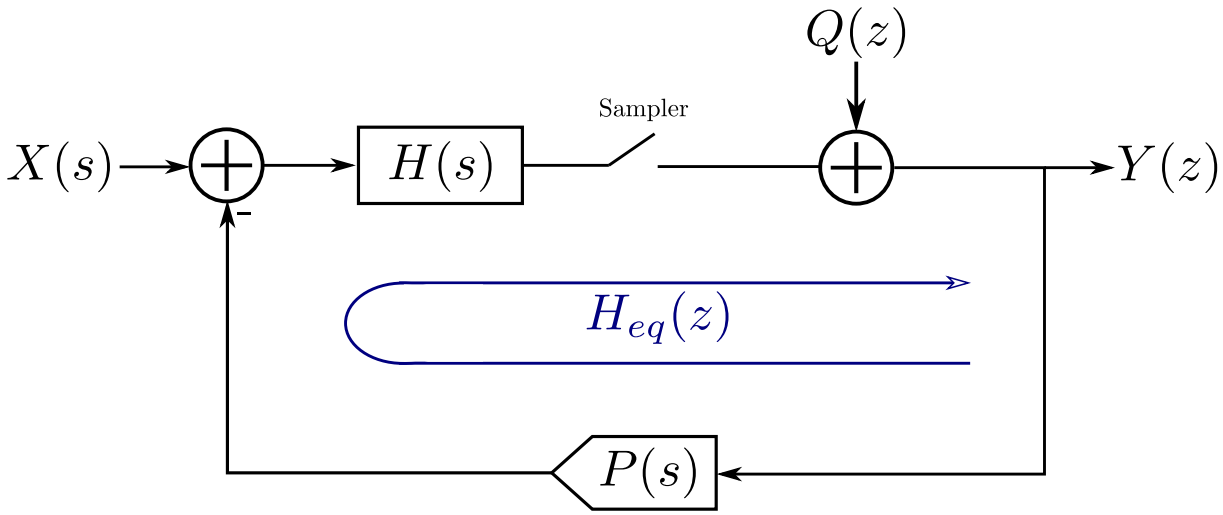


Figure 2.7: CT SDM.

A sketch of a CT SDM is given on figure 2.7. The input signal $x(t)$ with Laplace transform $X(s)$ is filtered by the CT loop filter $H(s)$, after which it is sampled and quantized to obtain the output signal. In the feedback path, the digital output signal $Y(z)$ is passed to a DAC to obtain an analog signal. The transfer function around the entire loop of the SDM is called $H_{eq}(z)$. This is also the loop filter that a DT SDM resulting in the same NTF would have, and takes into account the loop filter, DAC and sampling operation. It can be expressed as

$$H_{eq}(z) = [H(s)DAC(s)]^* \tag{2.11}$$

The star operator $*$

In the previous expression the star operator * was used, which represents the sampling operation. Its effects are illustrated for a signal $w(t)$

$$\begin{cases} w^*(t) = w(t)\sum_{-\infty}^{\infty}\delta(t-nT) \\ W^*(s) = \mathcal{L}(w^*(t)) = \sum_{n=0}^{\infty} w(nT)(e^{sT})^{-n} \end{cases} \tag{2.12}$$

This can also be expressed as

$$W(z) = \mathcal{Z}(\mathcal{L}^{-1}(W(s))|_{t=nT}) \tag{2.13}$$

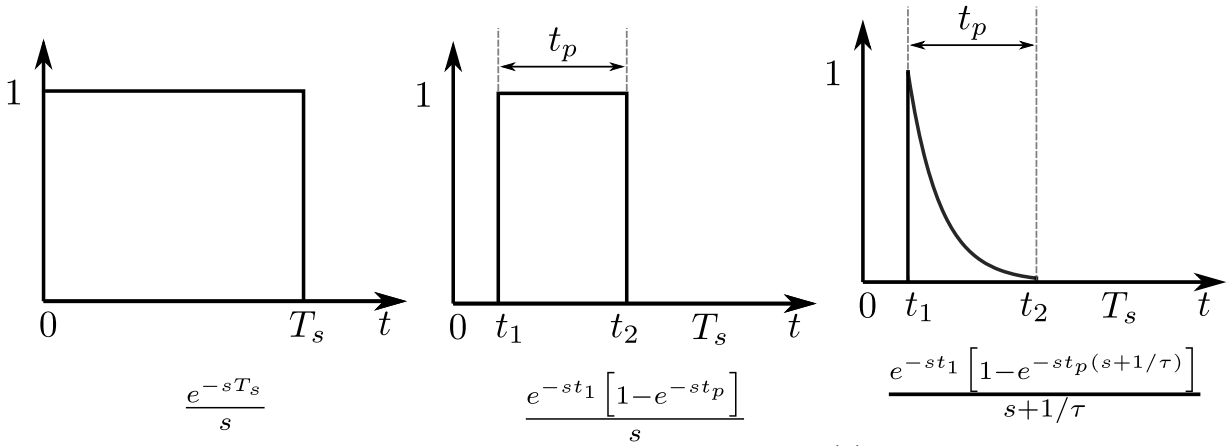
This is called the impulse-invariant transformation. Two important properties of the star operator are now introduced that will allow simplification of multiple expressions in the future.

$$\begin{cases} [A(s) + B(s)]^* = [A(s)]^* + [B(s)]^* \\ [A(s)B(e^{sT_s})]^* = [A(s)]^* B(z) \end{cases} \tag{2.14}$$

The first property indicates that the star operator is linear. Because discrete-time functions are expressed in the z-domain (with $z = e^{sT_s}$), the second property states that these expressions can be placed outside of the star operator. A more complete treatment of the star operator is provided in [6].

Digital-to-analog converters

DAC's are characterized by their impulse response. As an example, three of the most commonly used DAC pulses are shown on figure 2.8 along with their Laplace transforms. The most common pulse is the non-return-to-zero (NRZ) DAC. It is a rectangular pulse lasting the entire clock period T_s. It does not reset to 0, which explains its name, contrasting it with the return-to-zero or return-to-open (RTO) DAC. The switched-capacitor-resistor DAC is another commonly used pulse. The τ in its Laplace transform is the time constant of the exponential decay of a capacitor discharging through a resistor.



(a) NRZ pulse.

(b) return-to-open pulse.

(c) switched-capacitor-resistor pulse.

Figure 2.8: Plot of the impulse responses for different DAC pulses and associated Laplace transforms [3].

Anti-aliasing

One of the main advantages of the CT SDM is undoubtedly the implicit anti-aliasing filtering performed by the loop. In the DT SDM, a costly anti-alias filter is necessary, since the sampling is performed at the input, causing signal components with a multiple of the sampling frequency to alias in-band.

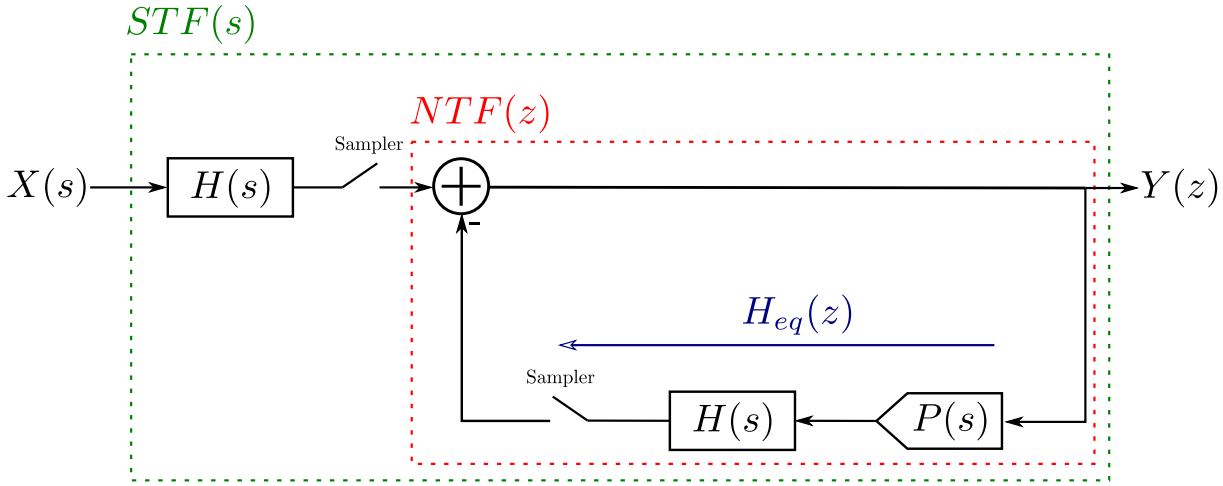


Figure 2.9: Redrawn CT SDM.

To demonstrate the anti-aliasing operation intuitively, the modulator is redrawn, placing the loop filter and sampler in front of the feedback node. The contribution of the input signal $X(s)$ to the output $Y(z)$ can be immediately determined as

$$Y(z) = \frac{1}{1 + H_{eq}(z)}[H(s)X(s)]^* = NTF(z)[H(s)X(s)]^* \tag{2.15}$$

Using the second property of the star operator, the following result is found as

$$Y(z) = [\underbrace{NTF(e^{sT_s})H(s)}_{\text{STF(s)}}X(s)]^* \tag{2.16}$$

At $f = 0$, pole-zero cancellation between $H(s)$ and $NTF(e^{sT_s})$ takes place, causing the unattenuated input signal to appear at the output. Frequencies at higher multiples of f_s that could cause aliasing, will be suppressed by the zeros of the $NTF(e^{sT_s})$ at these frequencies. This leads to a periodic pattern of notches in the the signal transfer function $STF(s)$ and provides excellent anti-alias behavior.

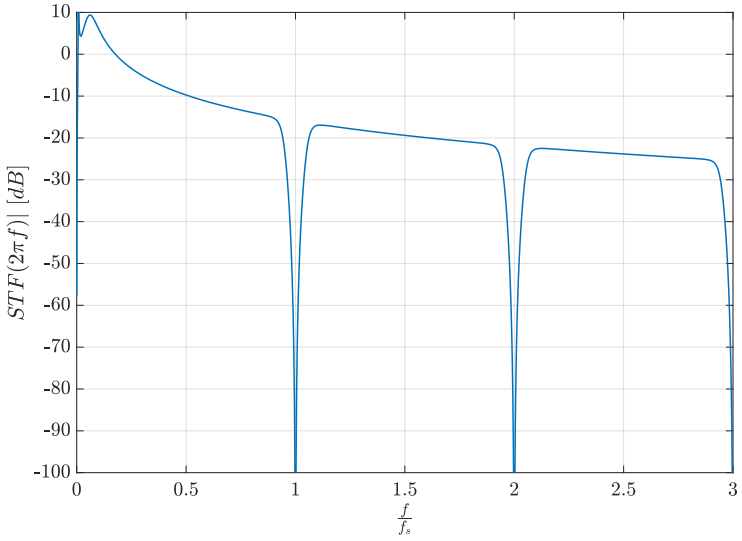


Figure 2.10: Example STF of a CT SDM.

2.2.3 One-bit sigma-delta modulators

For a long time, multi-bit SDMs were the standard. Using multi-bit quantization implies using multi-bit quantizers and DACs. Unfortunately, these are not entirely linear and this non-linearity will cause high-frequency quantization noise to modulate in-band. This is not a huge problem for the quantizer, as the NTF will suppress the errors introduced here. However, this is not the case for the DAC. A possible solution is using only a single bit as quantizer output. Single-bit quantization is inherently linear and allows for a very compact design as an added benefit. In this thesis, a single-bit quantizer will be used.

Chapter 3

Low-pass-filtering switched-capacitor DAC (LPSC DAC)

3.1 Motivation

It is now useful to analyse the simple CT SDM block diagram on figure 3.1, of which the error voltage at feedback node is denoted $\epsilon = X(s) - V_{fb}$. The CT loop transfer function $H(s)$ will be built using integrators. In this design these will be RC-active integrators, which are further discussed in chapter 5, and the current consumption of $H(s)$ will be dominated by the contribution of the first integrator. This can be understood as follows: the resistors in the integrators are generally sized to meet noise constraints. The input-referred noise caused by the resistors further in the filter will be suppressed by all preceding integrators, including the first, resulting in a progressively larger resistor sizing further in the loop filter. Since the current delivered by each of integrator opamps will be inversely proportional to the corresponding resistor and the first resistor must be the smallest, the first opamp will also deliver the largest current.

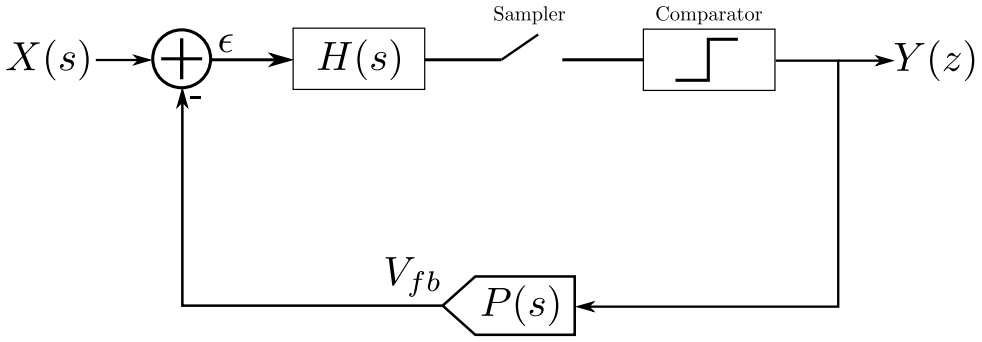


Figure 3.1: CT SDM with error signal ϵ.

This large current is proportional to the voltage ϵ. Due to the nullator operation of the loop feedback, the low frequency content of this signal will be almost zero, since the low-frequency content of V_{fb} will closely match $X(s)$ and these two contributions will cancel out. The greatest contributor to ϵ and thus the primary cause of the high current consumption, is unwanted high-frequency quantization noise present in V_{fb}. Introducing a filter in the feedback path will thus

allow this noise to be suppressed, greatly reducing the current consumption and requirements on the first integrator.

Though filtering in the feedback path can improve the current consumption without adverse effects, this has usually no positive impact on errors introduced by the DAC. After all, the filtering is usually performed in CT after the DAC, so the errors have already entered the system. However, performing the filtering in discrete-time before the digital-to-analog conversion has the potential to greatly reduce these errors. Many errors, such as jitter, cause high-frequency noise to modulate in-band and filtering in the DAC can suppress this noise before it influences the analog signal.

3.2 Analysis

A filter proposed to perform this filtering is displayed on figure 3.2.

It is called a low-pass filtering switched-capacitor (LPSC) DAC. It uses two non-overlapping clock signals ϕ_1 and ϕ_2. Their pulse widths are denoted by T_1 and T_2. Their sum is approximately equal to, but slightly smaller than the sampling clock period T_s: $T_1 + T_2 \lesssim T_s$. A short analysis of the LPSC DAC is presented. A sketch of the clock phases is shown on figure 3.3.

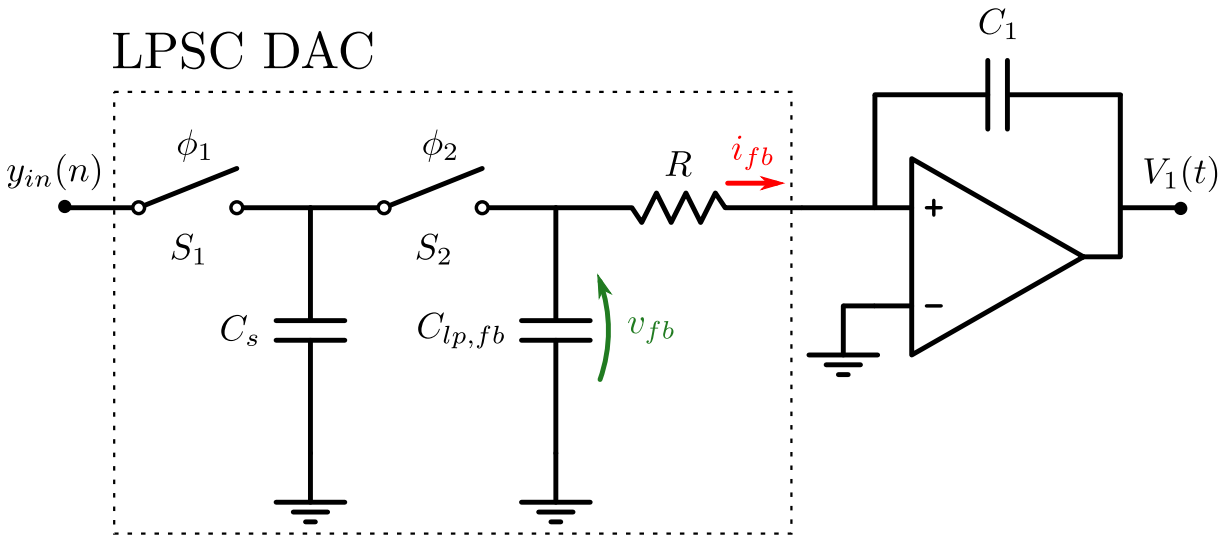


Figure 3.2: Feedback branch of the SDM with LPSC DAC and integrator.

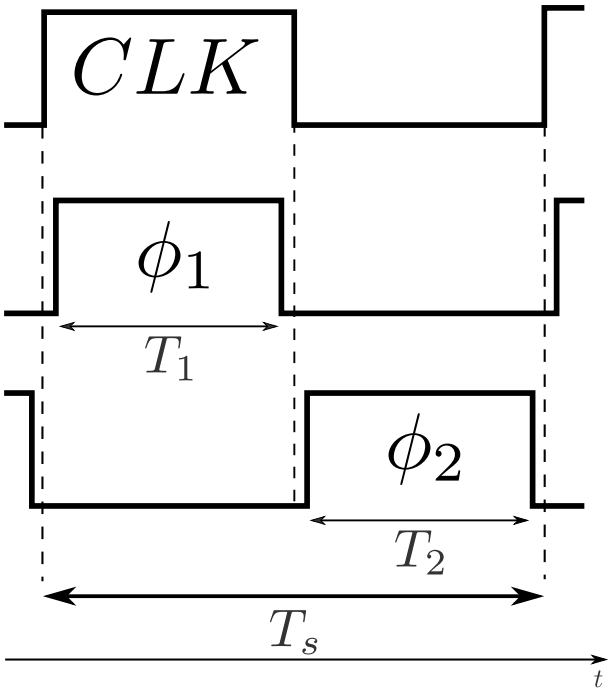


Figure 3.3: Sketch of the clock phases. Differences are exaggerated for clarity.

When ϕ_1 is high, C_s will either be charged to the high reference voltage $V_{ref+} = 1.2\ V$ or discharged towards the low reference voltage $V_{ref-} = 0\ V$ depending whether $y(n)$ is high or low respectively. The input voltage can thus be written as $y_{in}(n) = y(n)V_{ref+}$. When ϕ_2 is high, C_s and $C_{lp,fb}$ are placed in parallel and their charge redistributed. Using the conservation of charge principle, the voltages $v_{fb}(0-, n)$ and $v_{fb}(0+, n)$ just before and after the n-th rising edge of ϕ_2, are found to be

$$v_{fb}(0+, n) = \frac{C_{lp,fb}v_{fb}(0-, n) + C_s y_{in}(n)}{C_{lp,fb} + C_s} \tag{3.1}$$

The voltage $v_{fp}(t)$ will exponentially decay over a clock period, starting during ϕ_2. However, this decay is not equal during the two phases. During ϕ_2, C_s and $C_{lp,fb}$ are connected in parallel, and the time constant is thus $R(C_{lp,fb} + C_s)$. During ϕ_1, C_s is disconnected from the integrator and the time constant is simply $RC_{lp,fb}$. The decay over one clock period is then

$$\gamma = e^{-\frac{T_1}{RC_{lp,fb}}} e^{-\frac{T_2}{R(C_{lp,fb}+C_s)}} \tag{3.2}$$

We now introduce $\beta = \frac{C_s}{C_{lp,fb}+C_s}$ and find

$$\begin{cases} v_{fb}(0-, n) = \gamma v_{fb}(0+, n-1) \\ v_{fb}(0+, n) = \beta y_{in}(n) + (1-\beta)v_{fb}(0-, n) = \beta y_{in}(n) + (1-\beta)\gamma v_{fb}(0+, n-1) \end{cases} \tag{3.3}$$

$v_{fb}(0+, n)$ is now rewritten as $v_{fb}(n)$. The transfer function $H_{lp}(z)$ of the z-transform of the input $Y_{in}(z)$ to $V_{fb}(z)$ is readily found as

$$H_{lp}(z) = \frac{V_{fb}(z)}{Y_{in}(z)} = \frac{\beta}{1 - (1-\beta)\gamma z^{-1}} \tag{3.4}$$

The corresponding impulse response is shown on figure 3.4. The output signal of the DAC will be the current $i_{fb}(t) = \frac{v_{fb}(t)}{R}$ flowing through R. The total DAC impulse response $h_{DAC}(t)$ can be found as the convolution of the impulse response of the low-pass filter $h_{lp}(t)$ and the exponential pulse $p(t)$. Expressed in the Laplace domain:

$$H_{DAC}(s) = P(s)H_{lp}(z)|_{z=e^{sT_s}} \tag{3.5}$$

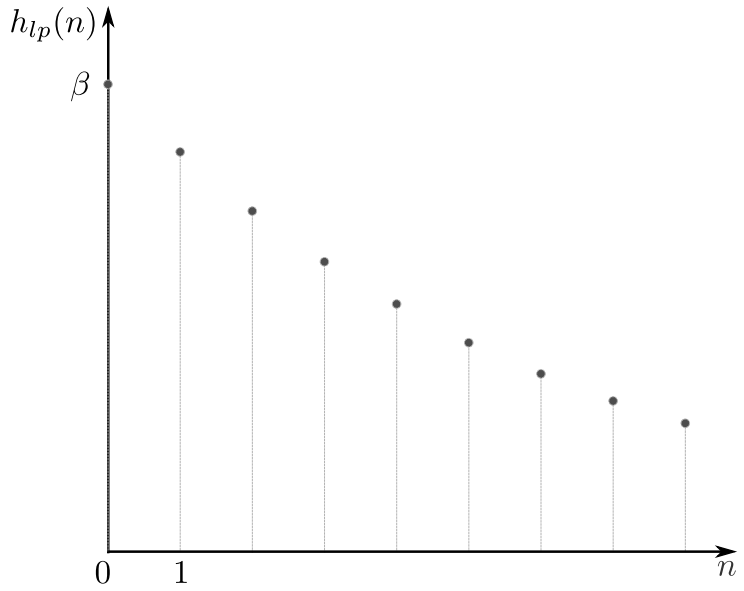


Figure 3.4: Impulse response $h_{lp}(n)$ of the LPSC DAC.

However, $p(t)$ and $P(s)$ must still be determined. It was previously mentioned that the time constants of the exponential decay during the two phases are slightly different. The total decay during one clock period can also be approximated as the result of a single exponential decay with time constant τ:

$$\gamma = e^{-\frac{T_s}{\tau}} \implies \tau = -\frac{T_s}{ln(\gamma)} = RC_{lp,fb}\frac{T_s}{T_s - \beta T_2} \tag{3.6}$$

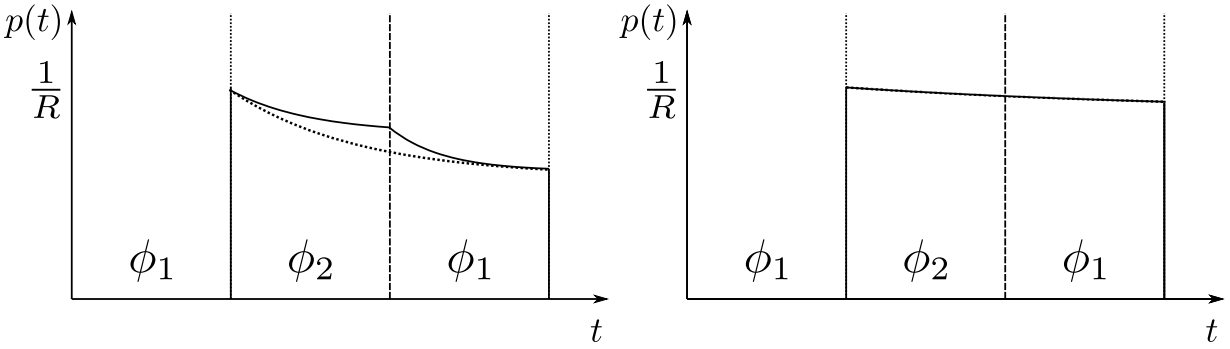
τ will be sized quite large to optimally filter the noise in the feedback path. However, care must be taken, as the noise introduced by R and the first integrator opamp will be amplified for too large τ when referred to the input of the sigma-delta modulator. This will be explained in-depth in the future. β will be small for reasons that will also be explained further in this text, leading to following simplification for τ, which will be very useful for the future sizing of $C_{lp,fb}$.

$$\tau \approx RC_{lp,fb} \tag{3.7}$$

The previously mentioned exponential pulse $p(t)$ starts during ϕ_2 and has a delay of T_1. As a consequence, it can be defined as follows

$$\begin{cases} p(t) = \frac{1}{R}e^{-\frac{t-T_1}{\tau}} & \text{for } T_1 \leq t < T_1 + T_s \\ p(t) = 0 & \text{elsewhere} \end{cases} \tag{3.8}$$

The approximated pulse from equation 3.8 and the real pulse are sketched on figure 3.5 for small and realistic τ. It is clear that equation 3.7 becomes a very good approximation for high τ. The total impulse response of the LPSC DAC is found by convoluting the discrete low-pass filter and the decaying exponential. It is shown on figure 3.6. Compared to the DACs discussed in subsection 2.2.2, the impulse response last longer than a clock period. This will lead to a reduced peak value, which is beneficial for slewing.



(a) Small value of τ **(b)** Realistic τ

Figure 3.5: sketches of the real (full line) and approximated (dashed line) pulse of the LPSC DAC for small τ (left) and realistic τ.

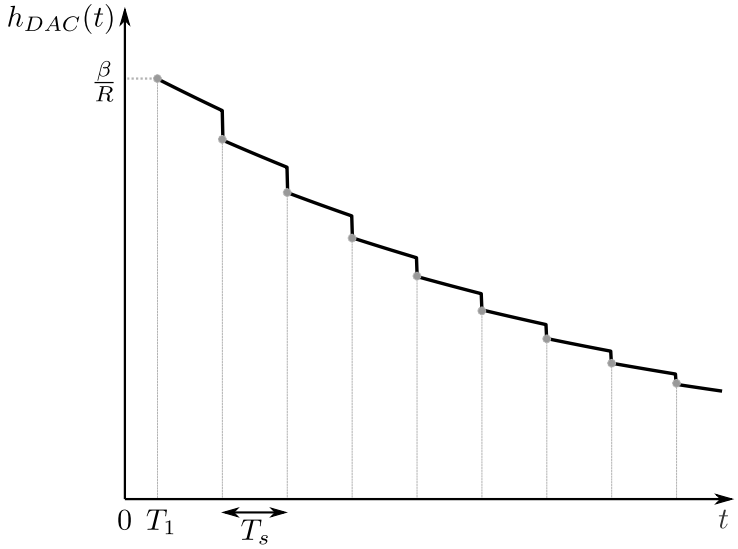


Figure 3.6: Total impulse response $h_{DAC}(t)$ of the LPSC DAC.

The Laplace transform $P(s)$ of the pulse is finally found as

$$P(s) = \mathcal{L}(p(t)) = \int_0^\infty p(t)e^{st}dt = \frac{e^{-sT_1}}{R}\int_0^{T_s} e^{-\frac{u}{\tau}}e^{su}du = \frac{e^{-sT_1}}{R}\left[-\frac{e^{-(s+\frac{1}{\tau})t}}{s+\frac{1}{\tau}}\right]_0^{T_s} \tag{3.9}$$

$$= \frac{1-\gamma e^{-sTs}}{s\tau+1}\frac{\tau e^{-sT_1}}{R} \tag{3.10}$$

With these expressions, the analysis of the LPSC DAC is now complete. Its transfer function can be expressed as the product of a continuous-time decaying exponential pulse $P(s)$ and a

discrete-time low pass filter $H_{lp}(z)$. This analysis out of the way, a system-level design using the LPSC DAC can be implemented and discussed in the next chapter. As a final illustration, the output waveform of an ideal LPSC DAC in one differential branch of the feedback path of the implemented SDM is included on figures 3.7 and 3.8.

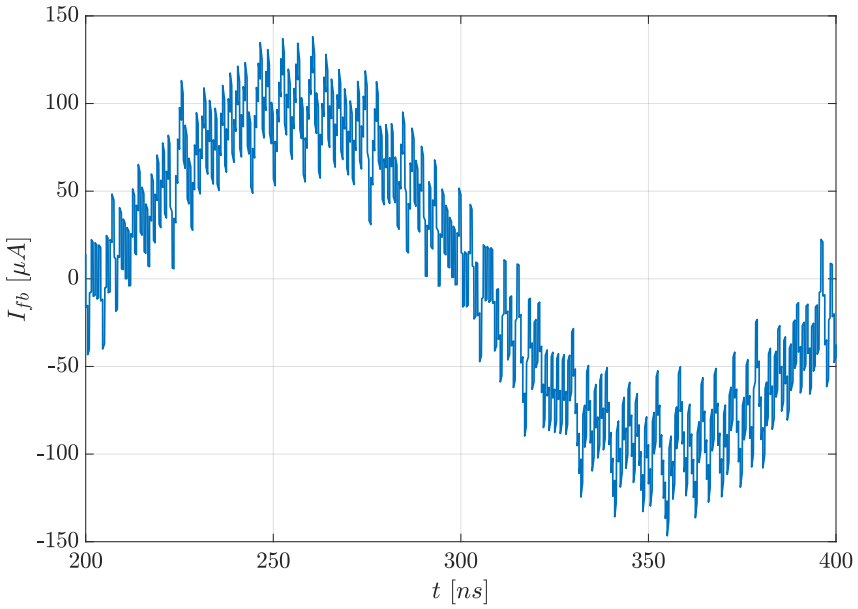


Figure 3.7: Example output current of the LPSC DAC in an SDM.

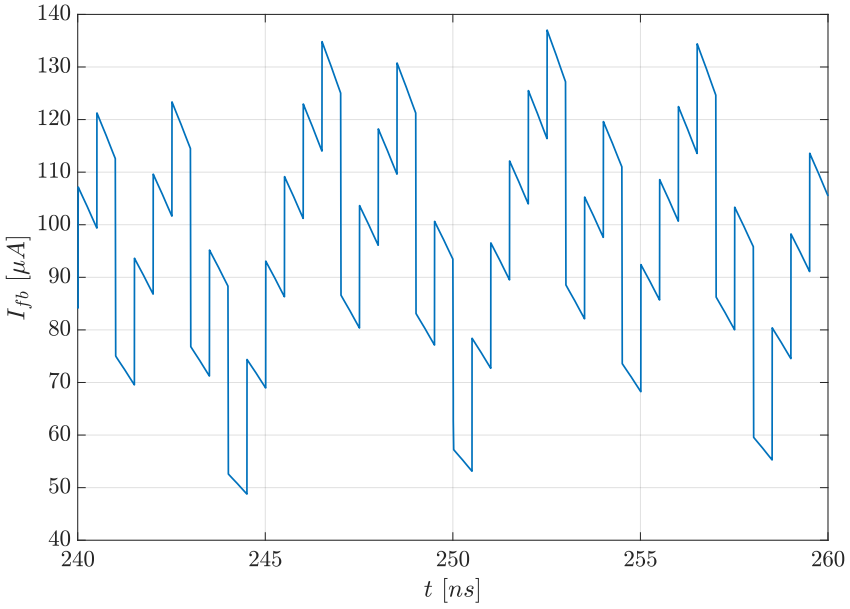


Figure 3.8: Output current zoomed in between 240 ns and 260 ns.

Chapter 4

System design

4.1 Compensation

The LPSC DAC has favourable properties, but its integration in SDMs faces a hurdle. Since its transfer function consists of the product of the low-pass filter $H_{lp}(z)$ and the exponential decaying pulse $P(s)$, this introduces an additional pole and will cause the order of the sigma-delta modulator to be raised by 1. Ideally, we'd like to design the NTF independently of the LPSC DAC. This can easily by accomplished by adding a compensating zero τ_c to the loop filter $H(s)$. In this case, a low-pass filter with a pole τ_c should be included in the input branch to restore the STF.

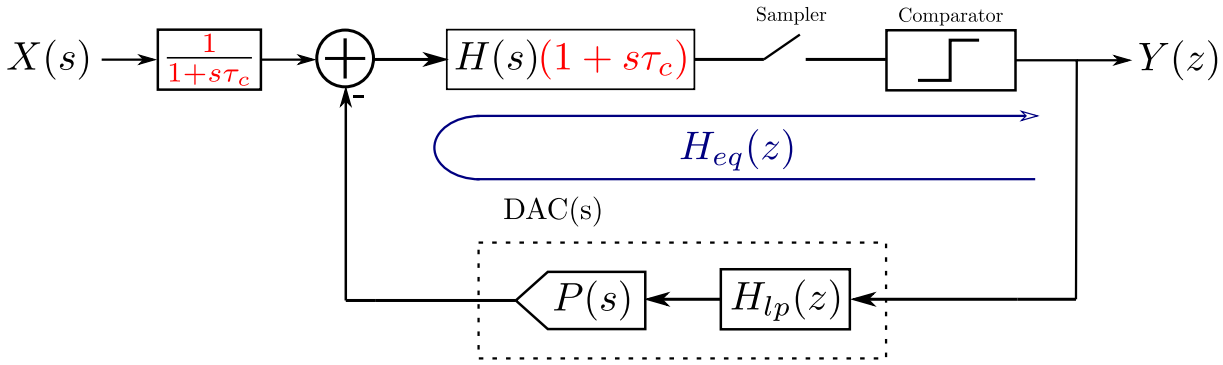


Figure 4.1: Proposed compensation of the LPSC DAC.

A simple example of the resulting structure is presented on figure 4.1. The LPSC DAC is visible in the feedback path. The continuous-time loop filter $H(s)$ is multiplied with $1 + s\tau_c$ (red) to obtain the compensating zero and the STF is restored by the pole in the input branch. The equivalent discrete-time loop filter $H_{eq}(z)$ is indicated in blue and expressed as

$$H_{eq}(z) = [H(s)(1 + s\tau_c)DAC(s)]^* \tag{4.1}$$

4.2 Specifications

The sampling rate of the implemented system is chosen as 2 GHz, resulting in a clock period of $T_s = 500\ ps$. The SDM is followed by multiple stages that decimate the output back to the original signal bandwidth. Each stage performs decimation with a simple factor, e.g. 2 or 3. Initially an OSR of 50 was selected, but taking into account the subsequent decimation, this was changed to 48. The output of the SDM can now easily be decimated by cascading 4 stages that decimate with a factor 2 and a stage that decimates with a factor 3. This OSR leads to a bandwidth of 20.83 MHz. The maximum out-of-band NTF gain is chosen as $||H_\infty|| = 1.5$ for stability, according to the empirical rule first formulated by M.L. Lee [7]. Higher values for $||H_\infty||$ are possible, but will lead to a lower maximum stable input amplitude. The simulations will be performed for a 5 MHz input signal of -6 dB relative to full scale (dBFS).

4.3 General model

In a first step, the LPSC DAC is integrated in a general SDM, in which the loop filter $H(s)$ is simply represented by a third-order CT transfer function. This will allow us to develop insight into the procedure to determine the compensating zero and loop filter coefficients without taking into account the internal structure of the loop filter, which would complicate these calculations. The noise transfer function $NTF(z)$ was designed in Matlab using the Delta-Sigma Toolbox developed by R. Schreier [8]. It can be found using the `SynthesizeNTF` function.
Based on the obtained NTF, the equivalent loop filter $H_{eq}(z)$ can be determined. The NTF and $H_{eq}(z)$ are given by

$$NTF(z) = \frac{(z-1)^3}{(z-0.6694)(z^2-1.531z+0.5539)} \tag{4.2}$$

The desired H_{eq} is then

$$H_{eq,des}(z) = \frac{1}{NTF(z)} - 1 = 0.79974\frac{(z^2-1.531z+0.5539)}{(z-1)^3} \tag{4.3}$$

The actual loop filter $H(s)$ is unknown, but is designed to be a third order filter of the form

$$H(s) = \frac{as^2+bs+c}{s^3} = \frac{a}{s} + \frac{b}{s^2} + \frac{c}{s^3} \tag{4.4}$$

The unknown coefficients of $H(s)$ can be found based on $H_{eq}(z)$, by taking into account the sampling operation and the transfer function of the DAC. Important here is also the added compensating zero $(1 + s\tau_c)$. Equations 4.1 and 4.3 will be combined to find the unknown loop filter coefficients a to c and the compensating zero τ_c.
Equation 4.1 can be simplified using the second property of the star operator in 2.14, after first splitting up the transfer function of the DAC in the continuous-time exponentially decaying pulse $P(s)$ and the discrete-time low-pass filter $H_{lp}(z)$. $H_{lp}(z)$ can be placed outside of the brackets.

$$H_{eq}(z) = \frac{1}{R}[H(s)(1+s\tau_c)P(s)]^* H_{lp}(z) \tag{4.5}$$

Substituting equation 4.1 in the previous expression results in

$$H_{eq}(z) = \frac{1}{R}[(\frac{a}{s} + \frac{b}{s^2} + \frac{c}{s^3})(1 + s\tau_c)P(s)]^* H_{lp}(z) = \frac{1}{R}[(a\tau_c + \frac{a + b\tau_c}{s} + \frac{bc\tau_c}{s^2} + \frac{c}{s^3})P(s)]^* H_{lp}(z) \tag{4.6}$$

Since the star operator is linear, each of the 4 terms can now be individually converted to expressions fully in discrete time by the impulse-invariant transformation, which will be performed in Matlab using the `c2d` function with the `impulse` option.

`c2d` performs a mathematically equivalent operation to equation 2.13 by using residue calculus, which is easier to implement in software. After this transformation, all terms are in the z-domain. After a few intermediary steps, the unknown coefficients can simply be determined by solving a system of equations. To avoid unnecessary repetition, this will not be discussed now, but be performed in the next section for the full system-level design.

4.4 Architecture

4.4.1 Overview

A second step was working towards a system-level design using integrator blocks. This design can easily be tested and translated to a design in Cadence. It is shown on figure 4.2 and based on the design in [9]. Its structure is a cascade of integrators with feedforward and feedback. From the feedforward topology it inherits a small internal signal swing at the first integrator, which will lead to better noise suppression and reduced constraints on the first integrator [4].

Three integrators form the loop filter $H(s)$ and are followed by a comparator and a sampler. Each integrator has an associated coefficient a to c. The compensating zero τ_c is integrated in the loop filter and compensated by a pole in front of the loop. The outer feedback path uses the previously described LPSC DAC, while the faster inner feedback path has an NRZ DAC. This dual feedback structure is beneficial for high-speed operation. Local feedback was introduced between the second integrator and the input, allowing the zeros of the NTF to be optimized to obtain a minimal amound of in-band noise. Because the noise-transfer function is a high-pass function, most of the in-band noise will be concentrated close to the band edge. Two complex conjugate zeros close to the band edge can suppress this noise. The optimal zeros are located at the normalized angular frequencies $\omega_z = 0$, $\omega_z = \sqrt{3/5}$ and $\omega_z = -\sqrt{3/5}$, leading to a signal to noise ratio (SNR) increase of 8 dB [10].

An input feed-in in front of the last integrator relaxes the requirements on the second integrator due to the inner loop. This can intuitively be understood as follows. Because the output of the DAC approximates the input signal, this path contributes a large low-frequency component to the input node of the third integrator. However, the input of each integrator should have a negligible low-frequency content. This can only be the case if the output of the second integrator has a very large low-frequency component, compensating the contribution of the DAC. The feed-in provides this large low-frequency component, therefore relaxing the requirements on the second integrator.

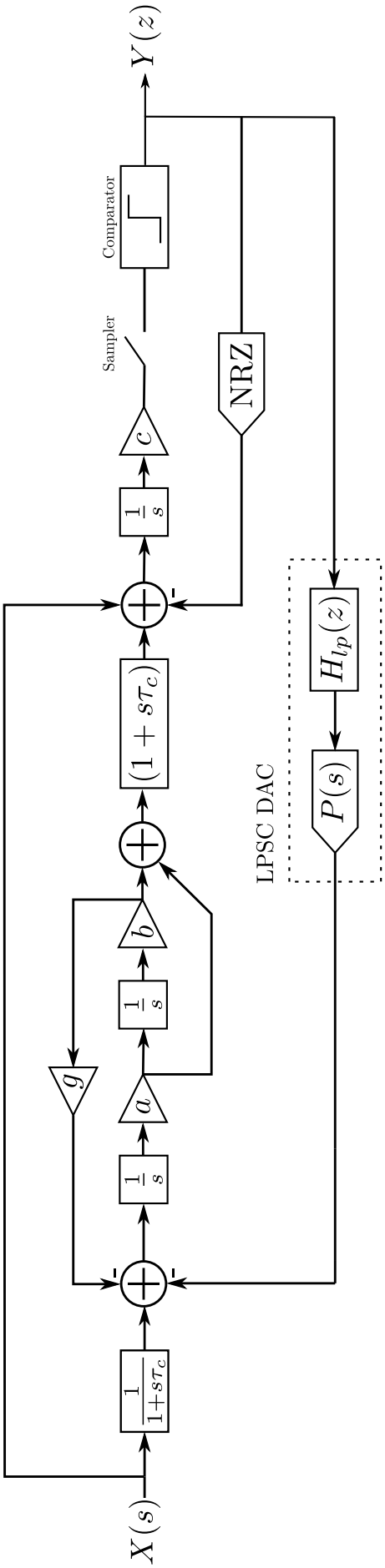


Figure 4.2: Total system-level design.

4.4.2 Determining the integrator coefficients and compensating zero

The procedure to find the integrator coefficients and compensating zero discussed in the previous section is now expanded for the architecture discussed in the previous section. This procedure is again fully performed in Matlab.

The addition of the local feedback will influence the expressions of both $H_{eq}(z)$ and $H(s)$ and requires a small change in calculation. The new expression for the desired $H_{eq}(z)$ is quickly found based on the NTF obtained by setting the zero optimization flag in `synthesizeNTF` to 1. It leads to

$$H_{eq,des}(z) = 0.79851\frac{(z^2 - 1.641z + 0.6964)}{(z-1)(z^2 - 1.998z + 1)} \tag{4.7}$$

The local feedback path with gain g is drawn separately on figure 4.3. The local feedback path itself is indicated in red. This leads to following transfer functions for the nodes $A(s)$ and $B(s)$, with $gab = \omega_z^2 = 3/5$:

$$\frac{A(s)}{\epsilon(s)} = \frac{as}{s^2 + \omega_z^2} \quad \& \quad \frac{B(s)}{\epsilon(s)} = \frac{as + ab}{s^2 + \omega_z^2} \tag{4.8}$$

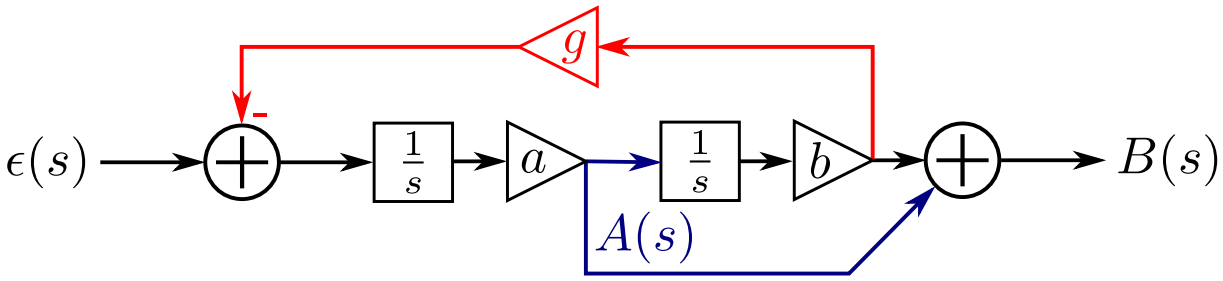


Figure 4.3: Local feedback path with gain g (red). Node $A(s)$ indicated in blue for clarity.

The fast inner feedback path with the NRZ DAC contributes a term that does not need to be transformed using the impulse invariant transformation. This path only contains an integrator term of which the $\mathcal{Z}$-transform is known to be simply $\frac{1}{z-1}$. In conclusion, summing all paths across the loop leads to a H_{eq} of the form

$$H_{eq}(z) = \left[(s\frac{ac\tau_c}{(s^2+\omega_z^2)} + \frac{ac + abc\tau_c}{(s^2+\omega_z^2)} + \frac{abc}{s(s^2+\omega_z^2)})P(s)\right]^* H_{lp}(z) + \frac{c}{z-1} \tag{4.9}$$

$H_{lp}(z)$ and $P(s)$ will depend on τ, which will be based on thermal noise considerations. This will be further discussed in section 5.2 and leads to $\tau = \frac{2}{5\pi f_b}$. The only remaining unknowns are thus a, b, c and τ_c. After performing the impulse invariant transformation on each term within

the brackets, $H_{eq}(z)$ will be of the form

$$\begin{aligned} H_{eq}(z) = \frac{1}{z-(1-\beta)\gamma}\Bigg[&\frac{(d(0.07475z+0.07075)}{z-1} \\ &+ \frac{e(0.01896z^2+0.1091z+0.01743)}{z^2-1.997z+1} \\ &+ \frac{f(0.003196z^3+0.07074z^2+0.06865z+0.002873)}{(z-1)(z^2-1.997z+1)}\Bigg] \\ &+ \frac{g}{z-1} \end{aligned} \tag{4.10}$$

With $d = ac\tau_c$, $e = ac + abc\tau_c$, $f = abc$ and $g = c$. The factor $\frac{1}{z-(1-\beta)\gamma}$ is the denominator of $H_{lp}(z)$. In Matlab, the terms in equations 4.10 and 4.7 can now be placed under a common denominator and equated. The polynomials in the numerators can be expressed as vectors, in this case by the coefficients of descending powers of z of the polynomial. The vector formed by the coefficients of the numerator of the desired $H_{eq}(z)$ forms the right side of the equation and is called RS. The numerator coefficients of the different terms of $H_{eq}(z)$ from equation 4.10 also form vectors and are joined in the matrix LS. The vector formed by the coefficients d, e, f and g can be found as

$$LS \cdot \begin{bmatrix} d \\ e \\ f \\ g \end{bmatrix} = RS \longrightarrow \begin{bmatrix} d \\ e \\ f \\ g \end{bmatrix} = \begin{bmatrix} 0.6734 \\ 1.5411 \\ 0.5117 \\ 0.0384 \end{bmatrix} = \begin{bmatrix} ac\tau_c \\ ac + abc\tau_c \\ abc \\ c \end{bmatrix} \tag{4.11}$$

These equations can be combined in the following quadratic equation, with $p = ac$

$$p^2 - fp + eg = 0 \tag{4.12}$$

There are two possible solutions to this equation. Both are result in the same NTF and STF and are equivalent. To select one, a reference CT design using an NRZ DAC was developed and the solution resulting in the best coefficient match with this design was chosen. Finally, all coefficients are obtained as

$$\begin{cases} p = 0.1762 \\ a = \frac{p}{c} = 0.2617 \\ b = \frac{f}{t} = 0.2177 \\ c = g = 0.0384 \\ \tau_c = \frac{d}{p} = 8.7466 \end{cases} \tag{4.13}$$

Chapter 5

Circuit design

5.1 Overview

In the following subsections, we'll be taking a closer look at the structures used to implement elements from the system-level design discussed in the previous chapter, such as the compensating zero and the local feedback. The total circuit is displayed at the end of the section on figure 5.6.
For the circuit implementation, a fully differential topology was chosen. Differential circuits are inherently robust against common-mode interference and parasitic effects, such as clock feedthrough in switches. Their signal swing is also doubled and inverting signals can simply be performed by cross-coupling the signal wires. A final advantage is that many analog building blocks (e.g. differential pairs) are usually inherently differential. Converting these circuits to a single-ended implementation will introduce parasitic poles and limit high-speed operation [5]. The circuits in the next subsections will be drawn in their single-sided equivalents for clarity.

5.1.1 Integrator

The main building block of the system, the integrators, will be implemented using active RC-integrators as shown on figure 5.1. Assuming a large enough opamp gain, the input terminals will act as virtual grounds due to the the negative feedback. In this case, the output V_{out} of the integrator can be approximated as

$$V_{out} = -\frac{1}{sRC}V_{in} \tag{5.1}$$

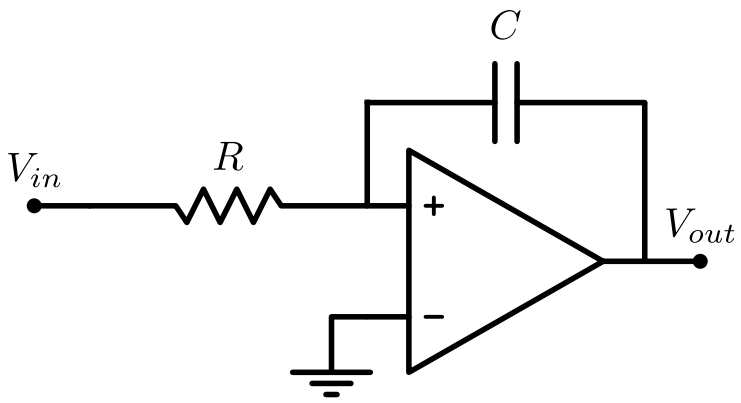


Figure 5.1: RC integrator.

5.1.2 Summing signals

Integrating a weighted sum of two signals V_1 and V_2 can now simply be performed by connecting them to the input terminals through two resistors R_1 and R_2. Such an integrator is displayed on figure 5.2. Its output is

$$V_{out,sum} = -\frac{1}{sR_1C}V_{in,1} - \frac{1}{sR_2C}V_{in,2} \tag{5.2}$$

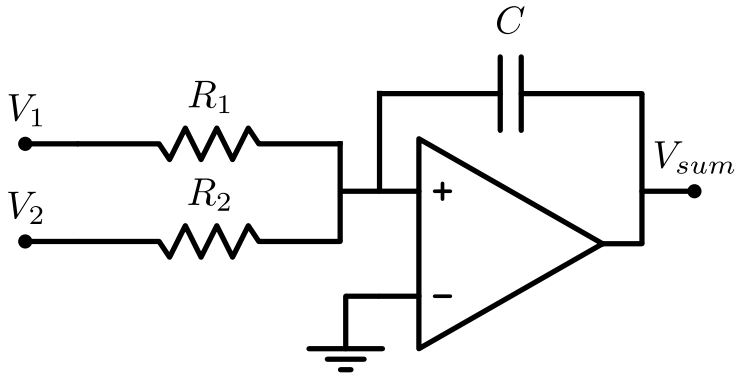


Figure 5.2: Integrated weighted sum of two signals V_1 and V_2.

5.1.3 Compensating zero

The compensating zero τ_c inside the loop filter is implemented by adding a parallel capacitor C_c to the resistors R_3 of the third integrator, which is displayed on figure 5.3. The contribution of these branches to the output $V_{out,3}$ of the third integrator is found as

$$V_3 = -\frac{sC_cR_3 + 1}{sR_3C_3}V_{in,3} = -\frac{s\tau_c + 1}{sR_3C_3}V_2 \tag{5.3}$$

Where $\tau_c = C_cR_3$. C_c can be freely chosen, which allows any value of τ_c to be obtained independently of the value of R_3.

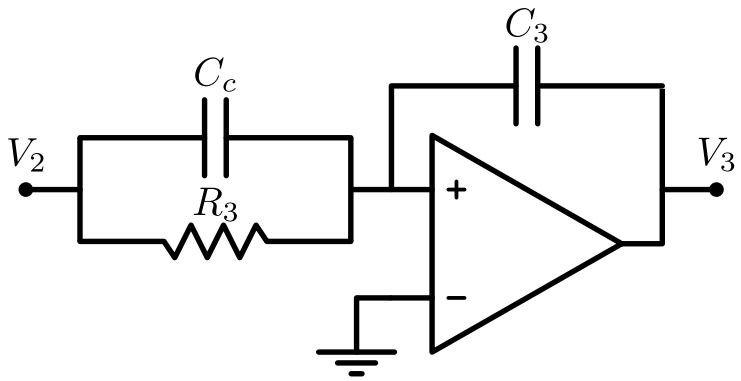


Figure 5.3: Integrator with compensating zero.

5.1.4 Pole in input branch

The extra pole in the input branch was is obtained by splitting the input resistance R_1 in 2 resistors $R_{1,a}$ and $R_{1,b}$ and adding a capacitance $C_{lp,in}$ to ground as shown on figure 5.4 In differential operation, $C_{lp,in}$ will actually be placed between the two differential signal lines. This means two capacitors to ground can be replaced by one capacitor half their size, resulting in a total capacitor area for $C_{LP,in}$ that is 4 times smaller. The output of the first integrator in function of the input is

$$V_1 = \frac{1}{sC_1(R_{1,a}+R_{1,b})}\frac{1}{1+sC_{lp,in}\frac{R_{1,a}R_{1,b}}{R_{1,a}+R_{1,b}}}X \tag{5.4}$$

The added pole must restore the transfer function of the forward path from V_{in} to V_{out}, so $R_{1,a}$, $R_{1,b}$ and $C_{lp,in}$ will be chosen in such a way to obtain

$$\tau_c = C_{lp,in}\frac{R_{1,a}R_{1,b}}{R_{1,a}+R_{1,b}} \tag{5.5}$$

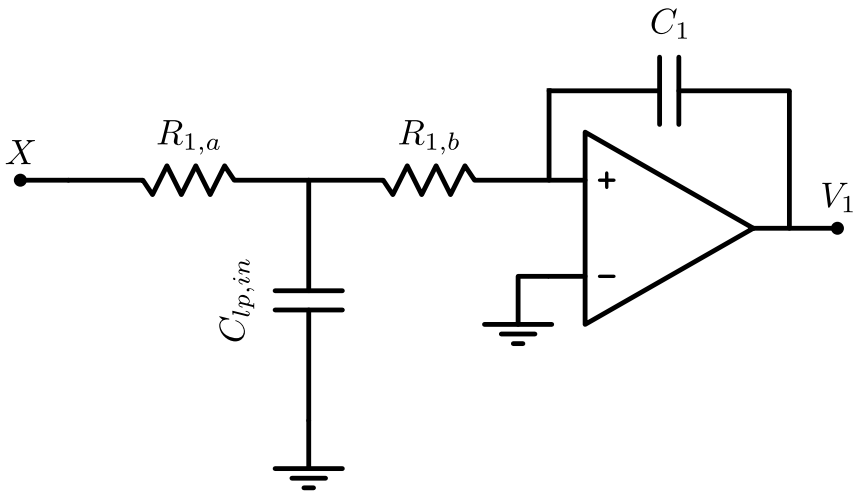


Figure 5.4: Integrator with low-pass filter in the input branch.

5.1.5 Local Feedback

The local feedback path is implemented using the feedback resistor R_g. This is shown on figure 5.5. Another look at the transfer function implemented by the local feedback reveals the following relationships:

$$\frac{V_1}{\epsilon(s)} = \frac{as}{s^2 + \frac{b}{R_g C_1}} \quad \& \quad \frac{V_2}{\epsilon(s)} = \frac{as + ab}{s^2 + \frac{b}{R_g C_1}} \tag{5.6}$$

From the system-level equation 4.8 and equation 5.6 it is clear that

$$\omega^2 = \frac{b}{R_g C_1} = \frac{b}{R_g C_1}\frac{R_1}{R_1} = \frac{abR_1}{R_g} \tag{5.7}$$

$$\Longrightarrow R_g = \frac{abR_1}{\omega^2} \tag{5.8}$$

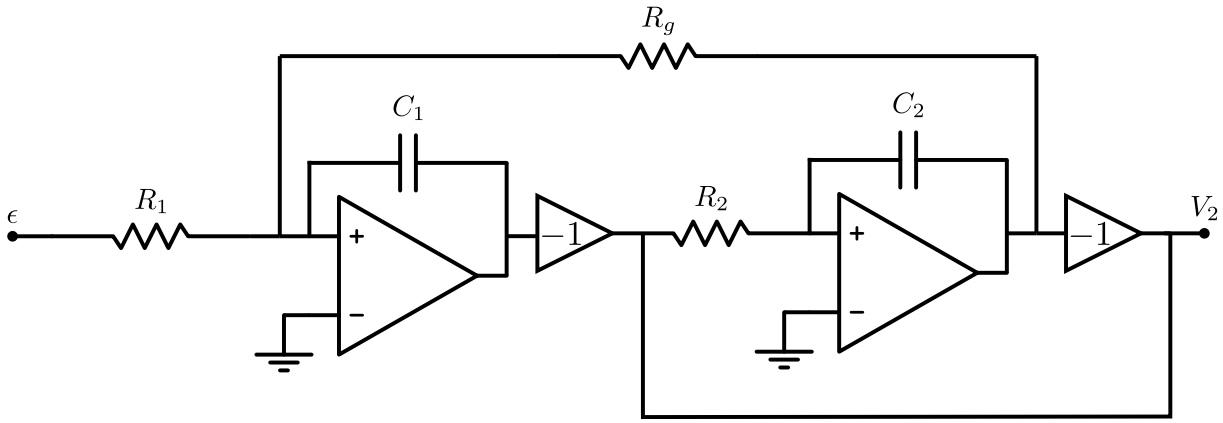


Figure 5.5: Paths with local feedback.

5.2 Determining the time constant τ

τ will be sized based on limitations of the input-referred thermal noise in the input and feedback branches. At low frequencies, the switched capacitor circuit around C_s in the LPSC DAC can be approximated as a resistor R_{eq}. R_{eq} is

$$R_{eq} = \frac{1}{f_s C_s} \tag{5.9}$$

C_s will later be sized based on the desired value for R_{eq}.

The input and feedback branch of the SDM at low frequencies are shown on figure 5.7, where resistors are replaced by ideal resistors and their Thévenin equivalent thermal noise sources V_{R_1} to $V_{R_{eq}}$. Seeing as the switched capacitor circuit around C_s can be reduced to a resistor R_{eq} at low frequencies, the entire LPSC DAC can be approximated as a low-pass filter. It is similar to the circuit of the input branch that was just discussed. The low-pass filter is of the form:

$$\frac{I_{out}}{V_{in}} = \frac{1}{R + R_{eq}}\frac{1}{1 + s\tau_c} = \frac{1}{R_1}\frac{1}{1 + s\tau_c} \tag{5.10}$$

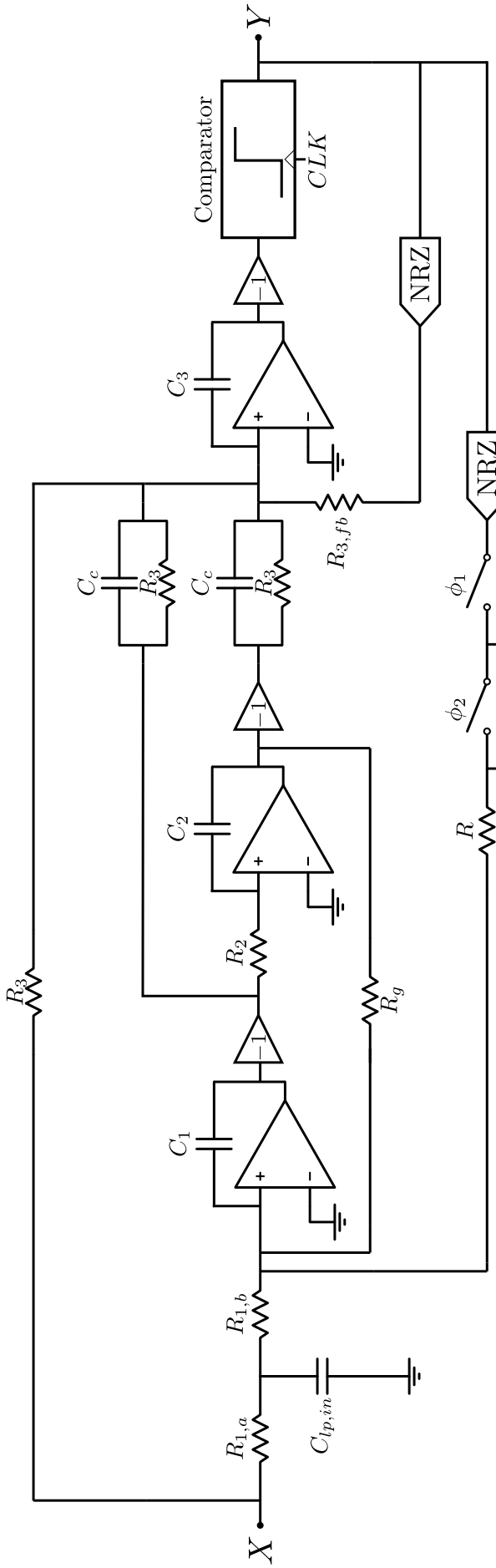


Figure 5.6: Total circuit-level design.

with

$$\tau_c = C_{lp,fb}\frac{RR_{eq}}{R+R_{eq}} \tag{5.11}$$

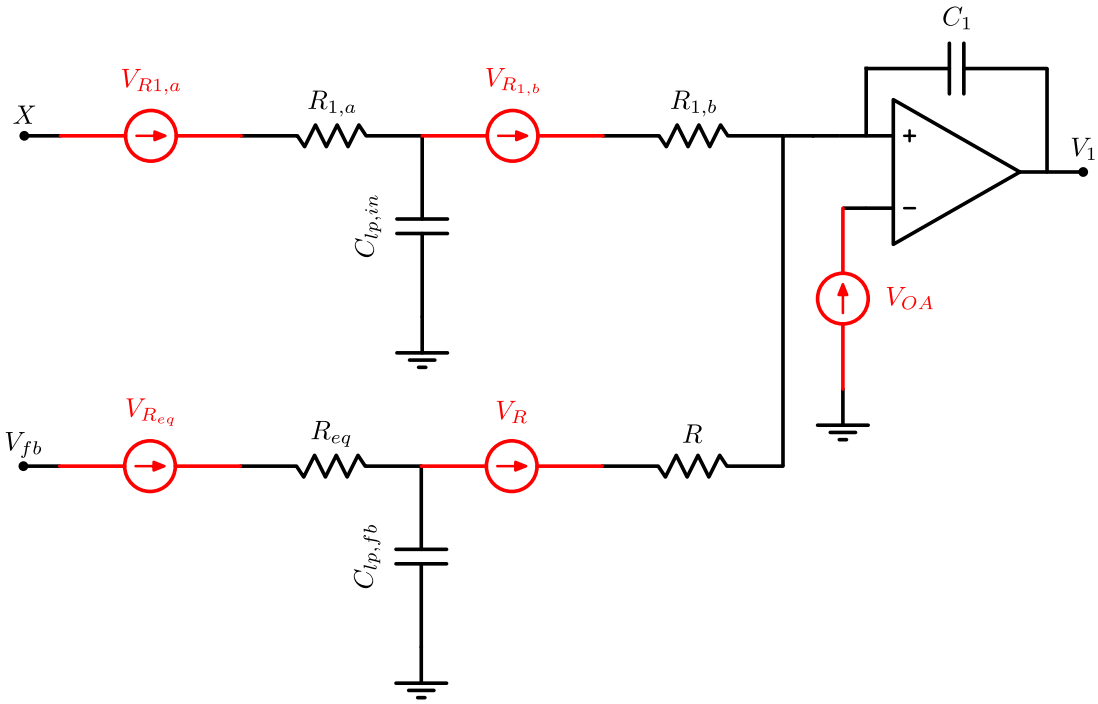


Figure 5.7: Low-frequency approximation of the input and feedback branches with added thermal noise sources (red).

We will assume τ to be sized relatively large ($\tau \geq T_s$). In this case, $\tau \approx RC_{lp,fb}$ and we can approximate τ_c as

$$\tau_c = C_{lp,fb}\frac{R\frac{1}{f_sC_s}}{R+\frac{1}{f_sC_s}} \approx \tau\frac{1}{RC_sf_s+1} \tag{5.12}$$

It is a well-known result in statistical physics that a resistor R generates white noise. Taking into account the differential nature of the circuit, the noise spectral density will be

$$S_R(f) = 8k_BTR \tag{5.13}$$

Where k_B is the Boltzmann's constant and T is the absolute temperature in Kelvin, which will be assumed to be 300 K.

The input-referred noise will then be determined via superposition of the different noise sources. The transfer functions from V_R and $V_{R_{1,b}}$ to I_{out} are

$$\frac{I_{out}}{V_R} = \frac{1}{R_1}\frac{s\tau+\frac{R_1}{R}}{s\tau+1} \quad \& \quad \frac{I_{out}}{V_{R_{1,b}}} = \frac{1}{R_1}\frac{s\tau+\frac{R_1}{R_{1,b}}}{s\tau+1} \tag{5.14}$$

In order to have an STF as close as possible to 1, the sum of R_{eq} and R must satisfy

$$R+R_{eq} = R_1 = R_{1,a}+R_{1,b} \tag{5.15}$$

The input-referred noise spectral density of the different contributions is now

$$\begin{aligned} S_{R,in}(s) &= 8k_BTR\left|\frac{R_1}{R}\frac{s\tau+\frac{R}{R_1}}{s\tau+1}(s\tau+1)\right|^2 + 8k_BTR_{1,b}\left|\frac{R_1}{R_{1,b}}\frac{s\tau+\frac{R_{1,b}}{R_1}}{s\tau+1}(s\tau+1)\right|^2 + 8k_BT(R_{eq}+R_{1,a}) \\ &= 8k_BT(\frac{1}{R}+\frac{1}{R_{1,b}})|R_1 s\tau|^2 + 8k_BT(R+R_{eq}+R_{1,a}+R_{1,b}) \\ &= 8k_BT(\frac{1}{R}+\frac{1}{R_{1,b}})|R_1 s\tau|^2 + 16k_BTR_1 \end{aligned} \tag{5.16}$$

The input-referred noise power due to the resistors is found as

$$P_{in,R} = \int_0^{f_b} S_{in}(s)|_{s=j2\pi f} df = 16k_BTf_bR_1\left(1+\frac{(2\pi f_b\tau_c)^2}{3}\left[\frac{R_1}{2R_{1,b}}+\frac{R_1}{2R}\right]\right) \tag{5.17}$$

In a similar vein, the input-referred noise of the opamp can be determined.

The noise of the opamp can be be represented by an equivalent noise source at the input that is mostly dominated by the input differential pair. Only the thermal noise will be taken into account. Calling α the effective number of transistors that contribute to the noise, the noise spectral density is

$$S_{OA}(f) = \gamma\alpha\frac{k_BTR}{g_m} \tag{5.18}$$

The factor γ lies between $\frac{1}{2}$ and 1, depending on how deep the transistor channels are inverted. It will be assumed that the integrator provides high in-band gain. The input-referred noise of the opamp can then be calculated similarly to the input-referred thermal resistor noise as

$$P_{in,OA} = \gamma\alpha\frac{k_BTf_b}{g_m}\left(1+\frac{(2\pi f_b\tau_c)^2}{3}\left[\frac{R_1}{2R_{1,b}}+\frac{R_1}{2R}\right]^2\right) \tag{5.19}$$

The goal of the LPSC DAC is to reduce the constraints on the first opamp, so we will assume the sizing of the opamp is limited by thermal noise considerations. In this case, it will generate an amount of thermal noise equal to the resistors, or $\frac{\gamma\alpha}{g_m} = 16R_1$. Based on equations 5.17 and 5.19, the time constant τ_c can be determined. It is clear that as τ_c increases, the low-pass filter will amplify the contribution of $R_{1,b}$ and R to the input-referred noise, and so τ_c cannot be sized too large. $R_{1,b}$, R, $R_{1,a}$ and R_{eq} will be chosen to be equal to reduce the size of $C_{lp,in}$ and $C_{lp,fb}$, which will already be quite large. τ_c will be chosen in such a way to obtain an increase of the input-referred thermal noise of no more than 1 dB. This results in $\tau_c = \frac{1}{5\pi f_b}$. Using equation 5.12, this leads to

$$\tau = \frac{2}{5\pi f_b} \tag{5.20}$$

5.3 Resistor sizing

As previously mentioned, the current delivered by the opamps will be inversely proportional to the resistors. Additionally, to maintain the same time constant, larger resistors will be associated with smaller capacitors, which is beneficial for bandwidth and slewing and reduces the

power consumption in the opamps. Ideally then, resistors would be sized as large as possible. Unfortunately, other considerations restrict this sizing, such as the minimal capacitor surface and the total surface of the resistors. By far the most important factor to consider, however, will be introduced noise.

In a first step, several noise sources will be added to the circuit, after which their transfer function to the output will be determined. The noise sources will consist of the noise introduced by the resistors and the input-referred noise of the opamps. In this analysis, only thermal noise will be considered, neglecting shot noise and 1/f noise. Afterwards, the transfer function from each noise source to the output will be determined. The system with added noise sources is shown on figure 5.8, with noise sources N_1 to N_3 in front of each integrator. The transfer functions of the noise sources to the output are found as

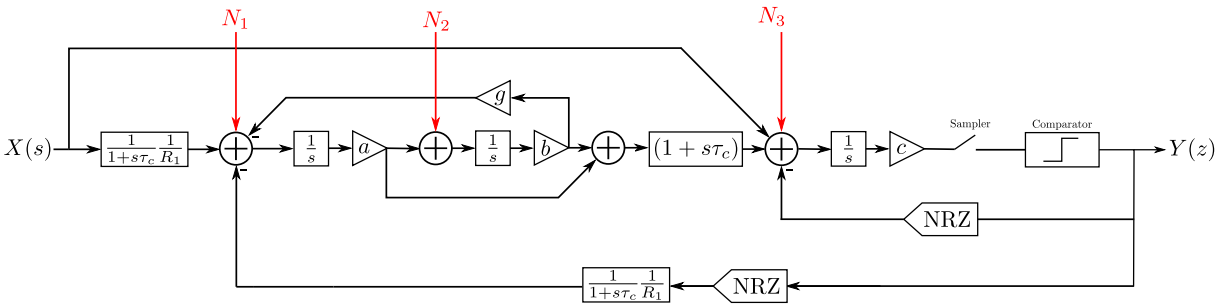


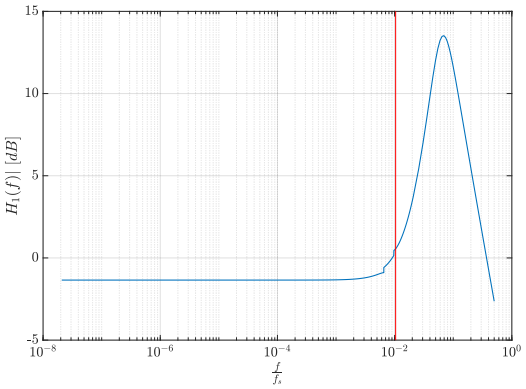
Figure 5.8: Added noise sources N_1, N_2 and N_3 in front of the integrators.

$$H_1(f) = \frac{V_{out}}{N_1} = NTF(z)\left[\frac{(as+ab)(1+s\tau_c)}{s^2+\omega_z^2}\frac{c}{s}\right] \tag{5.21}$$

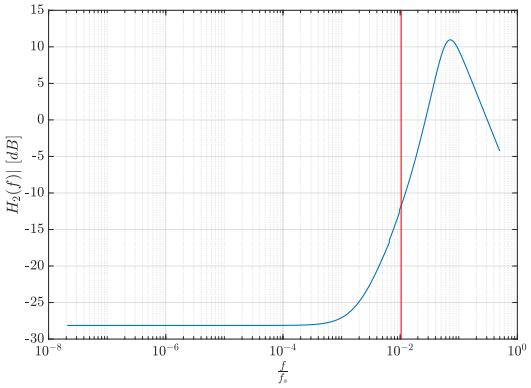
$$H_2(f) = \frac{V_{out}}{N_2} = NTF(z)\left[\frac{(bs-\omega_z^2)(1+s\tau_c)}{s^2+\omega_z^2}\frac{c}{s}\right] \tag{5.22}$$

$$H_3(f) = \frac{V_{out}}{N_3} = NTF(z)\left[\frac{c}{s}\right] \tag{5.23}$$

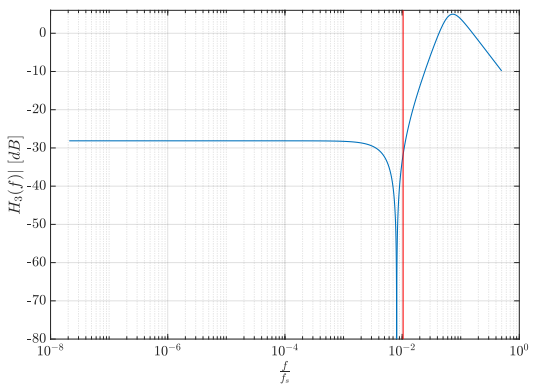
These transfer functions are plotted on figure 5.9. Small discontinuities are mathematical artifacts of pole-zero cancellation.



(a) $H_1(f)$



(b) $H_2(f)$



(c) $H_3(f)$

Figure 5.9: Transfer functions $H_1(f)$, $H_2(f)$ and $H_3(f)$. Bandwidth of the SDM in red.

From system simulations, an SNR of 82 dB was obtained for an input signal of -6 dB, placing the quantization noise floor at 88 dB. In SDMs, the thermal noise is often designed to be much higher than the quantization noise, since reducing thermal noise is very power consuming. Reducing the thermal noise in an SDM by a factor N means impedance scaling by the same factor. This leads to a power consumption that is roughly N times higher. Quantization noise is much easier to reduce, by for example increasing the aggressiveness of the NTF or adding an extra integrator, with a small additional cost in power consumption. As a rule of thumb, the thermal noise is set 12 dB higher than the quantization noise [4]. This means the thermal noise in this case is set at -76 $dBFS$. The resistors values R_1 to R_3 can now be found by calculating their in-band thermal noise power to the output and demanding it be less than a predefined level. The thermal noise of the resistors are calculated using equation 5.13, which takes into account the differential operation of the circuit.

Since the effect of the low-pass filter on thermal noise was designed to be negligible, N_1 consists of the thermal noise of R_{1a} to R_{eq} and the thermal noise of the first opamp, chosen to be as large as the thermal noise of the resistors. N_1 will be allowed to dominate the other thermal noise sources, as it is in comparison mostly unattenuated and reducing it would be

power consuming. It will be set at 77 dB and so

$$\frac{P_1}{R_1} = \frac{1}{R_3}\int_0^{f_b} |H_1(f)|^2 S_{N1}(f)df = -121\ dB \tag{5.24}$$
$$\implies R_1 = 3\ k\Omega\ \ \&\ \ R_{1a} = R_{1b} = R = R_{eq} = 1.5\ k\Omega$$

N_2 consists of the noise of R_2 and is more attenuated. It is set at 84 dB.

$$\frac{P_2}{R_2} = \frac{1}{R_3}\int_0^{f_b} |H_2(f)|^2 S_{N1}(f)df = -130\ dB \tag{5.25}$$
$$\implies R_2 = 20\ k\Omega$$

N_3 consists of the noise of R_3 and is even more attenuated. However, there are 4 branches with a resistor R_3 that must be taken into account. It is set at 86 dB.

$$\frac{P_3}{R_3} = \frac{1}{R_3}\int_0^{f_b} |H_3(f)|^2 S_{N1}(f)df = -142\ dB \tag{5.26}$$
$$\implies R_3 = 50\ k\Omega$$

The total thermal noise is then 76 dB. Based on the obtained resistor values, R_g can be determined using equation 5.8, which results in

$$R_g = 66\ k\Omega \tag{5.27}$$

Its noise will be assumed to be sufficiently attenuated.

5.4 Capacitor sizing

With the resistor sizing obtained in the previous section, the corresponding capacitors can immediately be sized based to obtain the desired integrator coefficients.

$$C_1 = \frac{1}{a}\frac{1}{f_{clk}R_1} = 637\ fF \tag{5.28}$$

$$C_2 = \frac{1}{b}\frac{1}{f_{clk}R_2} = 115\ fF \tag{5.29}$$

$$C_3 = \frac{1}{c}\frac{1}{f_{clk}R_3} = 14.9\ fF \tag{5.30}$$

Using the resistor values, τ and τ_c, the other capacitors are dimensioned as

$$C_s = \frac{1}{f_{clk}R_{eq}} = 333\ fF \tag{5.31}$$

$$C_{LP,FB} = \frac{\tau}{f_{clk}R} = 4.27\ pF \tag{5.32}$$

$$C_{LP,IN} = \frac{\tau_c}{f_{clk}\frac{R_{1,a}R_{1,b}}{R_{1,a}+R_{1,b}}} = 5.83\ pF \tag{5.33}$$

$$C_c = \frac{\tau_c}{f_{clk}R_3} = 87.5\ pF \tag{5.34}$$

5.5 Comparator

5.5.1 Introduction

The comparator is one of the main building blocks of the SDM. Initially, it was thought to be an uncritical component, but it will later be discussed that this is not the case. Specifications were a maximum offset $3\sigma \leq 50\ mV$ and a total current consumption of $I_{comp} \leq 100\ \mu A$.

The selected comparator was the classic StrongArm latch. It is displayed on figure 5.10. It is a compact comparator, boasting rail-to-rail outputs and zero static power consumption. The input-referred offset is also quite small and almost exclusively caused by a single differential pair [11]. As a result of its small noise bandwidth, the StrongArm latch also offers low input-referred noise. Aditionally, the StrongArm latch does not need any biasing, which makes for easier design compared to other options like the double-tail latch which are very sensitive to bias voltages [12][13].

The StrongArm operation is based on four distinct phases: a reset phase, sampling phase, propagation phase and regeneration phase. During the reset phase, the clock is low and the parasitic capacitances C_{int} and C_{out} at nodes *out* and *int* are charged to the analog supply voltage $V_{DD,a}$. During the sampling phase, CLK goes high and the tail transistor M_0 start conducting. In common-mode, this causes a current $I_0/2$ to flow in M_{1a} and M_{1b}. This current will discharge the capacitances C_{int} at the *int* nodes. During this phase, the differential input signal $V_{in} = V_{in+} - V_{in-}$ is amplified on the capacitances. The propagation phase starts when the common-voltage at *int* has decreased to $V_{DD,a} - V_{t,NMOS}$. M_{2a} and M_{2b} now start conducting and discharge nodes *out*. The differential output voltage $V_{out} = V_{out+} - V_{out-}$ will increase due to two contributions. A part of the differential current flowing through M_{1a} and M_{1b} is responsible for the first contribution. Additionally, the cross-coupled pair M_{2a} and M_{2b} act as a charge transfer device, redistributing charge integrated on C_{int} to C_{out}. At the end of the propagation phase, the common-mode voltage at *out* has reached $V_{DD,a} - |V_{t,PMOS}|$ and the PMOS transistors M_{3a} and M_{3b} turn on. This starts the regeneration phase, in which the NMOS and PMOS pairs form cross-coupled invertors and the positive feedback causes the differential voltage V_{out} to be exponentially amplified until it saturates. Finally, CLK goes low and the reset phase starts again[12][13].

Since the outputs of the StrongArm latch are connected to $V_{DD,a}$ during its reset phase, an additional component was necessary to maintain the output during the entire clock cycle. Usually, a simple set-reset NAND latch is proposed. For faster performance, another building block was used, drawing inspiration from the doctoral work of M. Verbeke [14]. This building block will be discussed in subsection 5.5.3.

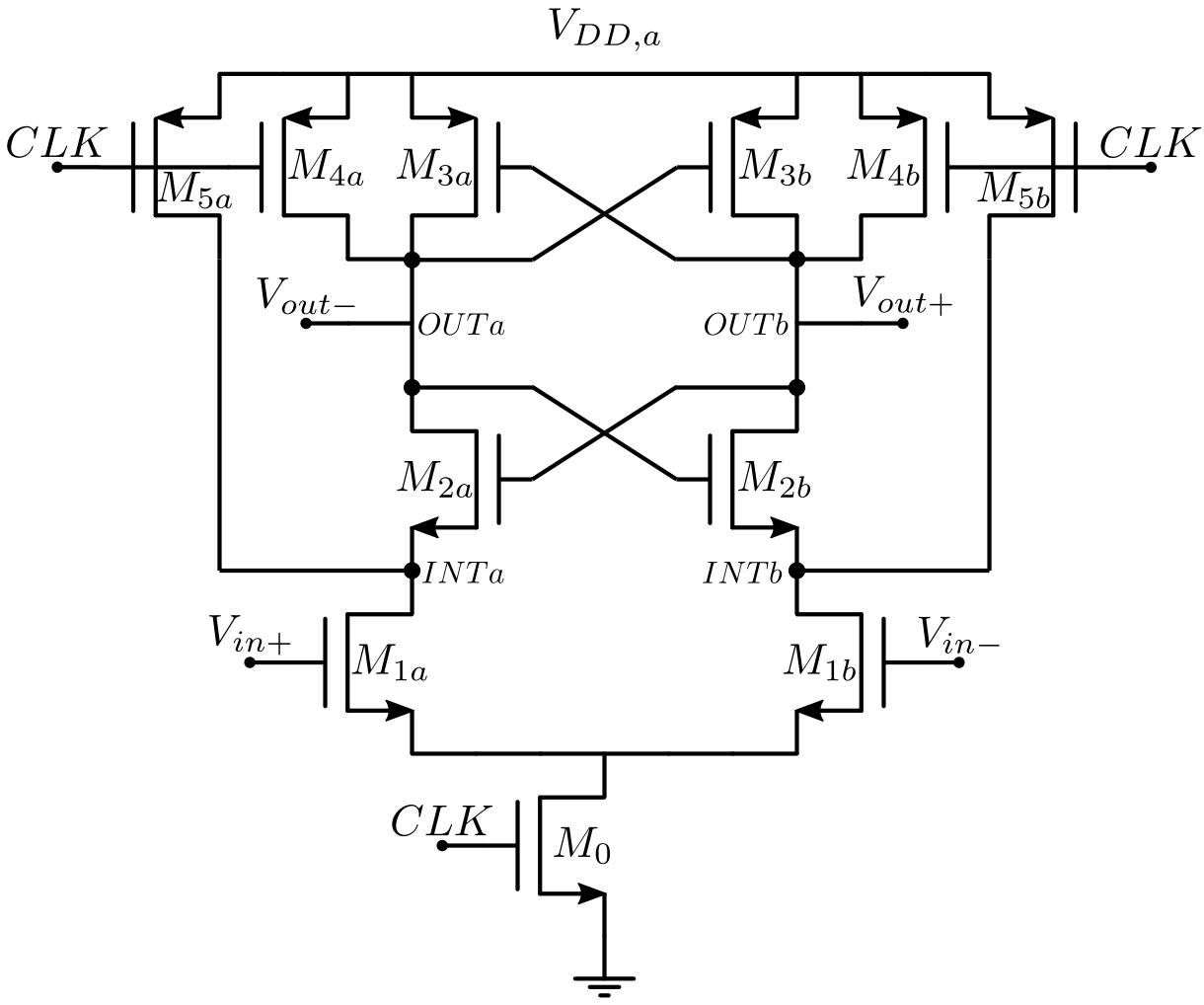


Figure 5.10: Circuit of the StrongArm comparator.

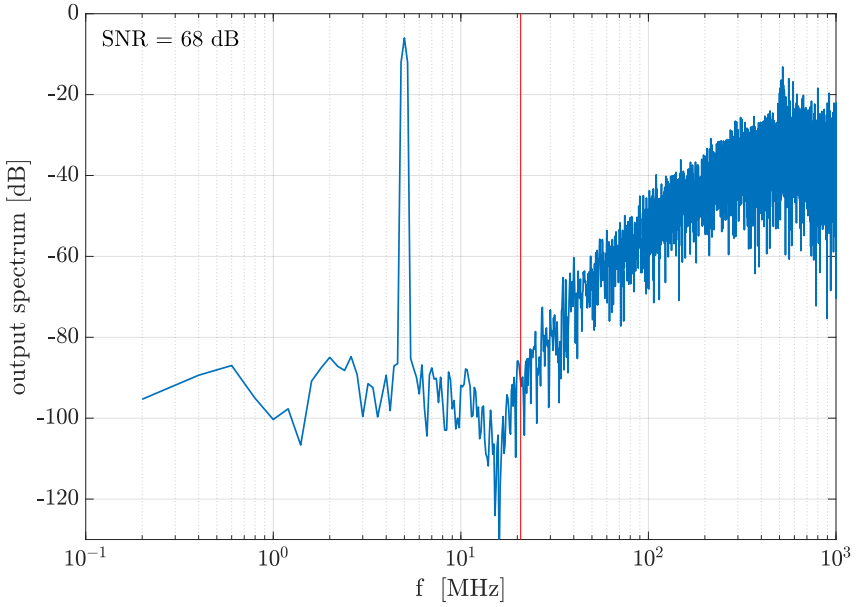
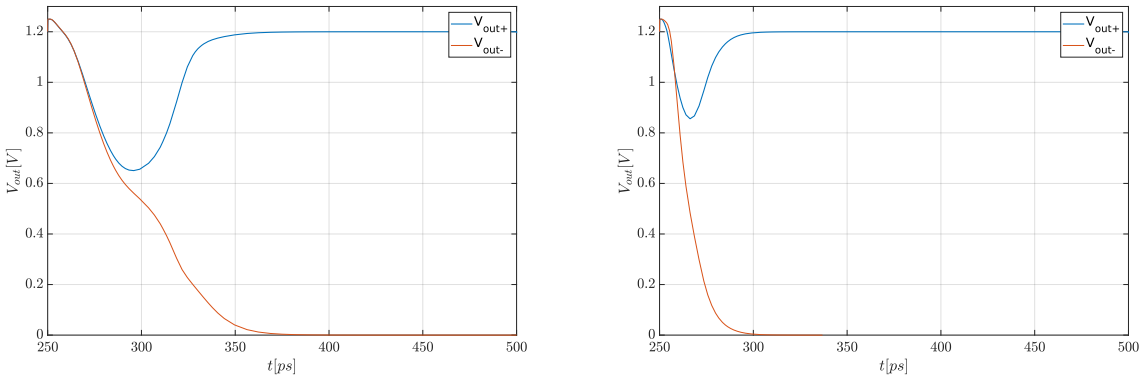


Figure 5.11: Output spectrum of an SDM affected by metastability in one of the first designs for a 5 MHz input signal of -6 $dBFS$. Bandwidth of the SDM in red.

5.5.2 SNR degradation

Once the first few implementations of the comparator were used in the actual SDM, problems arised. The comparator itself appeared to work as expected, with low offset and a large sensitivity, but a large SNR degradation was observed. This is shown on figure 5.11 for a simulation with ideal components except the comparator. The noise shaping had become second-order instead of third-order. However, the notch of the local feedback was still visible, indicating a correctly functioning outer loop. This insight allowed us to limit the search for possible problems to the inner loop. The first option that was investigated was a saturating output of the last integrator, which is known to cause such graceful degradation. In this case, the last integrator does not contribute to the noise shaping, but the first two integrators still do, resulting in a second-order sigma-delta modulator. After ruling out this possibility, it became clear that the problems were probably caused by the non-ideal comparator waveform.

Multiple tests were developed by examining the output of the real comparator and comparing it with an ideal output waveform. Deviations from the ideal output that could possibly lead to degradations were investigated. For each of these cases, the SNR was found using simulations performed with an ideal verilogA comparator with the added non-ideality, such as a large delay. Contrary to initial expectations the problem was not a fixed delay. Tests revealed other possible causes, such as limited or unequal rise and fall times at the output of the comparator, were not responsible for the SNR degradation either.



(a) Small input signal.

(b) Normally sized input signal.

Figure 5.12: Waveforms for differently sized input signals, where CLK goes high at 250 ps.

The cause was finally found to be comparator metastability, in which the regeneration time for small input signals is severely increased. This is a signal-dependent delay. As illustration, two waveforms are included on figure 5.12 for a small and a normally sized input signal. The signal-dependent delay will lead to a variable feedback each clock cycle and consequently cause errors. To test the impact of metastability, the previously mentioned ideal comparator was used, but an additional VerilogA block was written to provide realistic input-dependent delays to the comparator output. The results from this simulation confirmed that metastability was the cause of the observed SNR degradation.

5.5.3 Final Design

Fixed delay and pulse width

The signal-dependent delay of the comparator is caused by metastability. The feedback path via the LPSC DAC is mostly unaffected by this variable delay, as the only critical timing constraint is that C_s must be charged before ϕ_2. The delay thus only influences the inner path to the third integrator. The proposed solution for this problem is driving this path by a DAC pulse with a fixed delay of half a clock that also lasts half a clock cycle. At the time instants where there is no pulse, the DAC transistors are in cutoff. THis DAC is what is called a return-to-open (RTO) DAC. Due to the fixed half clock period delay, the comparator is sure to have made a decision when the RTO pulse is generated.

The circuit proposed to implement this operation is shown on figure 5.13. The inputs V_{in+} and V_{in-} will be driven by the outputs of two set-reset latches. Each set-reset latch maintains one of the outputs of the comparator over the clock period. V_{in+} will be coupled to the V_{out+} output of the comparator via a set-reset stage and V_{in-} similarly to the V_{out-} output of the comparator.

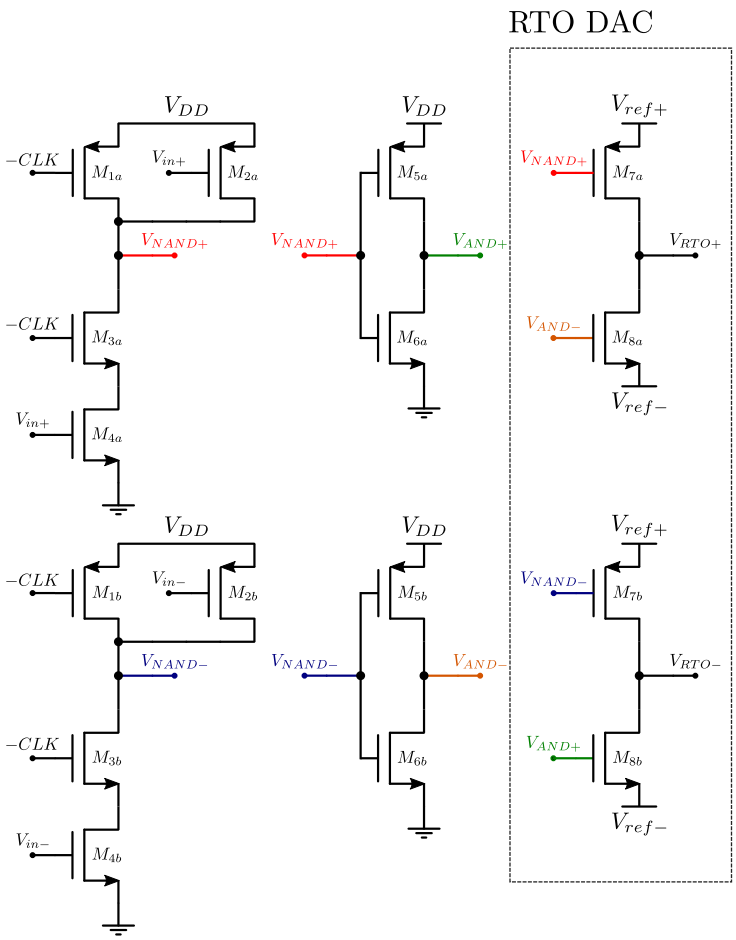


Figure 5.13: Circuit to realize the RTO pulse.

The following discussion will center on the output V_{RTO+} but a similar reasoning also valid for V_{RTO-}. If the clock signal CLK is low, this means the circuit is in the latter half of the clock period. In this case, V_{RTO+} should be pulled to V_{ref+} if the bit V_{in+} is high and pulled to V_{ref-} if V_{in+} is low. The NAND gate has two inputs, the inverted clock signal $-CLK$ and V_{in+}. If both are high, this means V_{in+} is high while the clock is low. In this case, the output V_{NAND+} of the NAND gate will be low. The output of the NAND gate drives the PMOS $M7a$, thus pulling the output V_{out+} towards V_{ref+} . If V_{in+} is low, V_{in-} will be high due to the operation of the differential circuit. In this case, V_{NAND-} will be low. This voltage is inverted by an invertor to obtain V_{AND-}, which will be high. This signal will drive the NMOS $M8a$, pulling the output V_{out+} down towards V_{ref-} as intended. The same reasoning can be repeated for V_{RTO-}. As long as CLK is high, the outputs of both NAND gates will be high and the NMOS and PMOS switches will be in cutoff. In this case, the circuit has no influence on integrator.

The NMOS devices are sized minimally in order to minimize power consumption and maximize speed. The PMOS devices are sized a factor 3 larger to obtain equal rise and fall times. This is summarized in table 5.1. A total power consumption of 8.0 μW for the digital circuit (not counting the RTO DAC) is obtained.

	W [nm]	L [nm]
M1, M2, M5	360	60
M3, M4, M6	120	60

Table 5.1: Transistor sizing

Unfortunately, this method means some tuning of the integrator coefficients is necessary to obtain the same transfer function. However, since this feedback path only contains one integrator, only the total feedback current through the resistor R_{3fb} of the third integrator over one clock period matters. Therefore, $R_{3,fb}$ must be halved to $R_{3,fb} = 25\ k\Omega$ to obtain the same injected current, since the feedback pulse only lasts half as long as originally envisioned. The RTO DAC and the sizing for M_7 and M_8 itself is further discussed in section 5.7.

Preamplifier

The StrongArm latch is quite sensitive to the input common-mode voltage V_{CM}. A too high V_{CM} might cause the input differential pair to enter triode region during the propagation phase, erasing the amplified voltage on the *out* nodes and degrading input-referred noise and offset due to lower gain. Additionally, this comparator suffers from the drawback of kickback, in which the high output variations couple back to the input through parasitic capacitances. To guarantee a correct common-mode input voltage and to isolate the preceding parts of the circuit from the voltage kickback a preamplifier was placed in front of the comparator in the initial designs of this circuit. The preamplifier is a simple differential PMOS pair with an active NMOS load and shown on figure 5.14.

The preamplifier output voltage $V_{out} = V_{out+} - V_{out-}$ can be found in function of the differential input $V_{in} = V_{in+} - V_{in-}$ as

$$V_{out} = \frac{-\frac{g_{m,1}}{g_{m,2}}}{1 + s\frac{C_{out}}{g_{m,2}}} V_{in} \tag{5.35}$$

This causes a problem. $\frac{g_{m,1}}{g_{m,2}}$ should be high to have decent DC amplification, however, $g_{m,2}$ should also be high in order to place the pole $\frac{g_{m,2}}{C_{out}}$ relatively high. Both of these conditions can only be fulfilled if either the current increases or the input differential pair of the comparator is made smaller, which also slows down the circuit. Additionally, the common-mode voltage at the output of the third opamp is already good, being a few tens of mV's higher than $V_{t,NMOS}$. As a consequence, there was no real need for the preamplifier circuit anymore and it was left out.

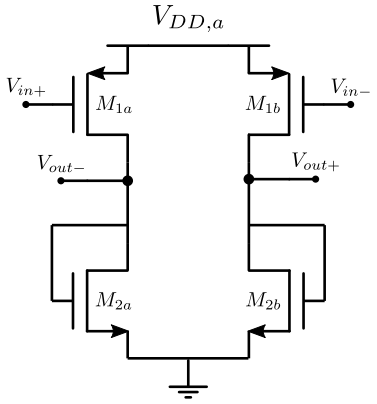


Figure 5.14: Preamplifier circuit.

Comparator

It is now instructive to perform a more quantitative analysis of the StrongArm comparator. We will be analyzing the speed of the different phases of the Strongarm operation. The sampling phase lasts as long as it takes to decharge node *int* by $V_{t,NMOS}$ and the MOSFETS M_{2a} and M_{2b} turn on. This phase lasts for

$$T_s = \frac{C_{int} V_{t,NMOS}}{\frac{1}{2} I_0} \tag{5.36}$$

The propagation phase ends when the PMOS transistors M_{3a} and M_{3b} turn on. This takes

$$T_p = \frac{(C_{int} + C_{out})|V_{t,PMOS}|}{\frac{1}{2} I_0} \tag{5.37}$$

During the propagation phase, the cross-coupled invertors will provide positive feedback. The net transconductance of one invertor will be called G_m. The output voltage $V_{out}(t)$ in this phase is exponentially amplified until M_2 and M_3 and can be found as

$$V_{out}(t) = V_{out,initial} e^{\frac{G_m}{C_{out}} t} \tag{5.38}$$

Where the regeneration time constant $\tau_{reg} = \frac{C_{out}}{G_m}$. Contrary to how transistors are usually sized in invertors, the PMOS transistors of the cross-coupled invertors will be sized equal to the NMOS transistors. This can be intuitively understood by noticing that both will contribute to the regeneration. However, the PMOS transistors will introduce more capacitance to C_{out} to obtain the same transconductance, as they must be sized larger due to the lower carrier mobility of the holes. An equal sizing will thus allow for a faster regeneration for the same transistor area and capacitance. Further decreasing of the PMOS size is not advised, since at the beginning of the regeneration phase, only the PMOS transistors contribute to the regeneration. Taking a closer look at regeneration time constant, it is found that

$$\tau_{reg} = \frac{C_{load} + C_2 + C_3}{G_m} \tag{5.39}$$

Where C_2 is the capacitance due to M_2 and C_3 the capacitance due to M_3.

	W [um]	L [nm]
M0	9	60
M1	5.8	60
M2, M3	1.8	60
M4	0.4	60
M5	0.2	60

Table 5.2: Transistor sizing for the comparator

Since the PMOS and NMOS transistors will be sized equally, $C_2 = C_3 \sim WL$ and $G_m \sim \frac{W}{L}$. It is immediately clear that to minimize τ_{reg}, L must be chosen as small as possible. It is also clear that as long as $C_2 + C3$ does not dominate C_{load}, it is beneficial to increase the width of M_2 and M_3. Beyond that point, the increase in transconductance G_m will be offset by the increase in the total output capacitance C_{out}. This will increase the area and power consumption in exchange for minimal benefits. It is chosen to have $C_2 + C3 = 5C_{load}$. The output nodes out_a and out_b will each be loaded with 2 PMOS transistors from the set-reset stages with $W = 360\ nm$, so for M_2 and M_3 the width is $W = 1.8\ \mu m$.

From equations 5.36 and 5.37, the benefit of a large I_0 and a large input differential pair is clear. A large input differential pair will also be beneficial for the input-referred offset voltage. M_0 operates in triode and will be sized in such a way not to significantly reduce I_0. We will require:

$$\frac{I_0}{2} = 300\ \mu A \tag{5.40}$$

The transistors M_4 and M_5 are sized large enough to charge the *out* and *int* nodes during the reset phase. The sizing for the comparator is summarized in table 5.2. This sizing leads to a power consumption of 62.1 μW for the comparator itself.

To determine the input-referred mismatch contributions, the reasoning in [13] is followed. Because M_2 and M_3 are only active during a part of the time, their contribution will be reduced. When they turn on, the signal has already been sufficiently amplified for their input-referred offset voltage to become negligible. Additionally, β mismatch of M_2 during the propagation phase has no influence at all, since in this phase the currents are set by the differential pair M_1. The input-referred offset voltage is thus dominated by the input differential pair. Using Pelgrom parameters [15] fitted to other technology nodes, $K_{V_T} = 3mV\ \mu m$ and $K_\alpha = 0.007\ \mu m$, we find

$$3\sigma = 3\sqrt{2\Big(\frac{K_\alpha}{\sqrt{W_1 L_1}}\frac{V_{Dsat}}{2}\Big)^2 + 2\Big(\frac{K_{V_T}}{\sqrt{W_1 L_1}}\Big)^2} = 22\ mV \tag{5.41}$$

Which is clearly good enough and provides some margin to eventual contributions of M_2 and M_3.

set-reset stage

The used circuit consists of two PMOS input transistors and a current mirror. It is displayed on figure 5.15. If the input V_{in-} of the right PMOS $M1b$ is low, the node V_{out} is pulled towards V_{DD}. If the input V_{in+} of the left transistor $M1a$ is low, the input voltage of the current mirror at node $mirr$ is pulled towards V_{DD}. In this case, a current will flow, which will be mirrored by $M3$. V_{out} will thus reach ground. During the reset stage of the StrongArm, the outputs of the comparator are charged to $V_{DD,a}$ and both PMOS transistors are cut off. The voltage is then sampled on the capacitance of the output. Both input voltages of the stage are not allowed be low, as in this case the output voltage cannot guaranteed to be be close to 0 V or V_{DD}, but will depend on the strength of the NMOS $M3$ and the PMOS $M1b$. This is not a problem, as these inputs can never be generated by the comparator.

Since the output V_{out} follows V_{in+}, two of these stages are used to maintain the two outputs of the comparator over the clock period: one stage with V_{out+} of the comparator at the V_{in+} input and V_{out-} at the V_{in-} input and the other stage with these inputs switched.

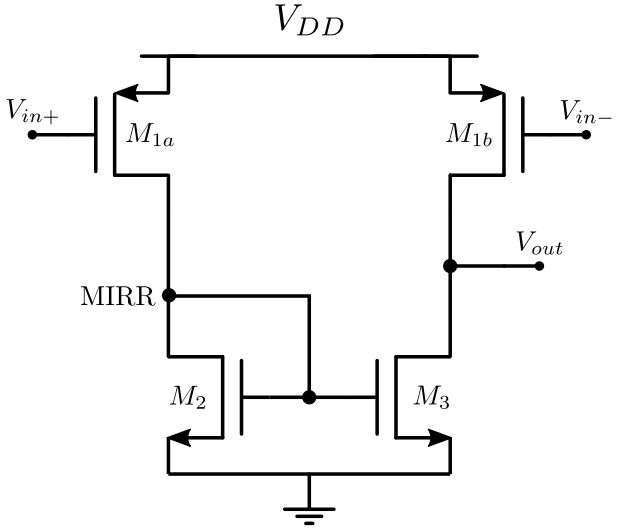


Figure 5.15: set-reset stage.

For the design of this digital stage, the classic flow for digital circuits will be followed, in which the circuit is analysed as an RC-network [16]. Of particular interest in digital electronics is the propagation delay: the time difference between the time at which the input of a circuit reaches half its final value and the time at which the output of a circuit reaches half its final value. This is usually approximated by simplifying the input voltage as a voltage step. For a capacitor C charging through a resistor R, $V_{out} = (1 - e^{-\frac{t_p}{RC}})V_{DD}$. The propagation delay t_p is then found as

$$\frac{V_{DD}}{2} = (1 - e^{-\frac{t_p}{RC}})V_{DD} \Longrightarrow t_p = ln(2)RC \tag{5.42}$$

The capacitances are the parasitic capacitances at each node, which will usually be domi-

nated by the gate capacitances. In the range relevant to the propagation delay, the transistors are in saturation modeled as an equivalent resistance R. For a minimally sized $NMOS$ transistor with drain current I_D and voltage V_D, this is obtained by simulation to be approximately

$$R = \frac{1}{-V_{DD}/2} \int_{V_{DD}}^{V_{DD}/2} \frac{V_D}{I_D} dV_D \approx 30\ k\Omega \tag{5.43}$$

We are now ready to tackle the sizing of the set-reset stage. M_2 is chosen minimally to reduce gate capacitance and power consumption. The PMOS transistors M_{1a} and M_{1b} are chosen 3 times larger as is usual in digital circuits, to take into account the different carrier mobility and obtain an equal equivalent resistance. The equivalent resistance of M_{1a}, M_{1b} and M_2 is called R.The question is now how to size M_3.

The propagation delay from V_{in-} to the output is, with C_{out} the capacitance at the output

$$t_{p,V_{in-}} = ln(2)RC_{out} \tag{5.44}$$

Now the propagation time from V_{in+} will be determined. The NMOS M_2 will turn on when the voltage at $mirr$ has increased to $V_{t,NMOS}$. This is

$$t_{mirr} = ln\Big(\frac{V_{DD}}{V_{DD} - V_{t,NMOS}}\Big) RC_{mirr} \tag{5.45}$$

M_3 will be sized a factor n larger than M_2. In this case, $C_{mirr} = (1+n)C_{M_2}$. The equivalent resistance of M_3 will then be $\frac{R}{n}$. The total propagation delay is then

$$t_{p,V_{in+}} = ln\Big(\frac{V_{DD}}{V_{DD} - V_{t,NMOS}}\Big) R(1+n)C_{M_2} + ln(2)\frac{R}{n}C_{out} \tag{5.46}$$

There are now two possible strategies to size n. Both are independent of the actual value of R. Either we minimize $t_{p,V_{in+}}$ or we choose it equal to $t_{p,V_{in-}}$. Depending on the output capacitance, the last strategy might not be possible and the additional delay associated with turning on M_3 cannot be overcome by increasing n. If the equation can be solved, there will be two solutions. In that case the most intelligent choice is probably choosing the smallest n to obtain approximately equal rise and fall times. We will choose the more general approach of minimizing $t_{p,V_{in+}}$. C_{out} will be dominated by the gate capacitances of the subsequent stages, the LPSC DAC driver from subsection 5.6.3 and one NAND gate from the circuit to generate the RTO pulse of subsection 5.5.3. Each of these consists of one minimally sized NMOS and a PMOS sized 3 times larger. In conclusion, $C_{out} = 8C_{M_3}$ and we find $n = 3$.

The sizing for the transistors in this stage are shown in table 5.3. The power consumption of one stage is 15.6 μW, but since 2 are used, this is 31.2 μW. The total power consumed in the comparator and subsequent set-reset stages is then 31.2 μW + 62.1 μW = 93.3 μW, almost exactly what was allocated.

	W [nm]	L [nm]
M1	360	60
M2	120	60
M3	360	60

Table 5.3: Sizing for the set-reset stage.

5.6 LPSC DAC

5.6.1 Switches

Many of the circuits described in the following sections will act as switches, so a short discussion on MOSFET switches is in order, based on [5].
Due to their small drain-source voltage, MOSFET switches will operate in the linear/triode region. The conductivity of a PMOS transistor in triode can be approximated by

$$G = \frac{dI_{DS}}{dV_{DS}}|_{V_{DS}\approx 0} = \frac{d\frac{W}{L}\mu C_{ox}(V_{GS} - V_{T,PMOS} - \frac{V_{DS}}{2})V_{DS}}{dV_{DS}}|_{V_{DS}\approx 0} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_{T,PMOS}) \tag{5.47}$$

The expression for an NMOS in triode is similar. Clearly these conductances depends on V_{GS}, but these expressions are actually only a rough approximation. In reality the conductance will be very non-linear. The voltage at the source will be the input voltage V_{in}. To turn on an NMOS switch, a high gate voltage is used and a low gate voltage is used for the PMOS. These are constant, so the conductance will depend on V_{in}. From equation 5.47, it is clear that PMOS transistors will conduct much better for high input voltages. The opposite is true for NMOS transistors. In fact, NMOS transistors only conduct for $V_{in} < V_{DD} - V_{T,NMOS}$ and PMOS transistors for $V_{in} > |V_{T,PMOS}|$.

There are also two parasitic dynamic effects. When a conducting transistor is switched off, the charge present in the conducting channel will be redistributed towards the source and drain. If the clock switches quickly, half of the charge will be directed towards the source and half towards the drain. The second parasitic effect is the coupling of the switching clock to the source and drain due to the parasitic gate-source and gate-drain capacitances. However, this is a signal-independent common mode effect that is cancelled in differential operation.

5.6.2 Transmission gate S_2

Since C_s and $C_{lp,fb}$ will be exchange charge during ϕ_2 and reach a common voltage, S_2 must be able to pass voltages over the full voltage range. Therefore, using a simple NMOS or PMOS switch will not be sufficient. Instead a CMOS switch or transmission gate is used, in which a PMOS and NMOS are placed in parallel. The conductivity of such a switch is $G_{s_2}(V_{in}) = G_{PMOS}(V_{in}) + G_{NMOS}(V_{in})$. Associated with this conductivity is the on-resistance of the switch $R_{s_2}(V_{in}) = \frac{1}{G_{s_2}(V_{in})}$. Again, the conductivity and associated resistance are not

constant at all over the voltage range, which will cause the current-voltage relationship to be non-linear and cause distortion. In order to reduce the influence of this non-linearity, the W/L ratio of the MOSFETs can be increased. However, this will increase the parasitic capacitance introduced by the switch, especially the highly non-linear junction capacitances.

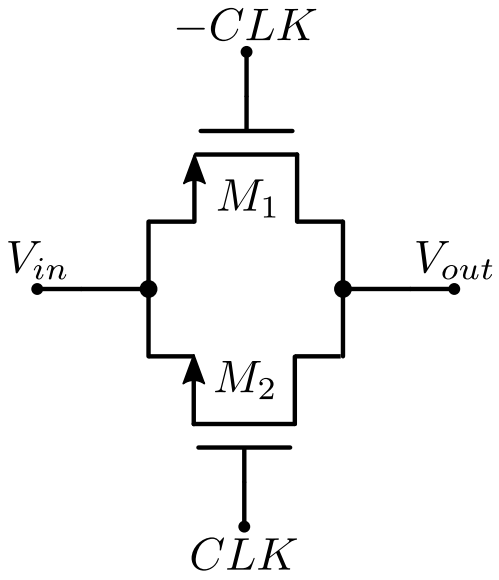


Figure 5.16: CMOS switch or transmission gate.

For the switch dimensions, there are two main concern: speed and linearity. In a first step, it will be assumed the switch has a constant resistance value R_{s2}, and an upper bound on this resistance will be determined for sufficiently fast operation. Since this is a continuous-time signal, the time wherein the two capacitors C_{LP} and C_s exchange charge is of critical importance. In the ideal case, this process is instantaneous, but the presence of the switch will introduce delay. It is possible to analyze this by approximating C_{LP} as a voltage source and to determine the charging or discharging of C_s towards its final voltage. However, this does not take into account the discharge through the resistor R. For a more accurate modeling, the differential equations governing one branch of the differential circuit with an LPSC DAC are solved. The voltage at the input of the first opamp is called V_{CM} and the voltage over C_s is called V_s.
The differential equations are given by

$$C_s \frac{dV_s}{dt} = -\frac{V_s - V_{fb}}{R_{s2}} \tag{5.48}$$

$$C_{lp,fb} \frac{dV_{fb}}{dt} = \frac{V_s - V_{fb}}{R_{s2}} - \frac{V_{fb} - V_{CM}}{R} \tag{5.49}$$

The larger voltage the difference between V_s and V_{fb} at the beginning of ϕ_2, the larger the introduced delay will be. The worst-case difference is $0.8\ V$. It will be demanded that the actual voltage V_{fb} over $C_{lp,fb}$ reach within 1% of the ideal voltage within 50 ps in this worst-case scenario. This was performed numerically in Matlab and results in $R_{s2} = 65\ \Omega$.

	W [um]	L [nm]	Remarks
M1	27.5	60	LVT
M2	9.2	60	LVT

Table 5.4: Optimal sizing for S_2

Though this sizing gave good results with constant switch resistances, the non-linearity of real transmission gates led to large harmonics in the sigma-delta modulator output spectrum. Even order harmonics are suppressed by the differential operation and all harmonics after the third fall out of band for the presupposed 5 MHz input signal. Of interest is thus the third harmonic distortion (HD3). To minimize the distortion, the following procedure is followed. First, we will require that $R_{s_2}(V_{in} = 1.2\ V) = R_{s_2}(0\ V)$ to maximize the linearity over the entire input voltage range. We will be using low treshold voltage transistors to reduce the resistance. Afterwards, the MOSFETS will be increased in size to reduce the effect of resistance non-linearity until a maximum signal to noise and distortion ratio (SNDR) or minimal HD3 is reached. Beyond this point, any decrease in resistance non-linearity will be offset by an increase of the non-linear junction capacitances. The optimal sizing was obtained by simulation and is shown in table 5.4. It results in

$$R_{s_2}(V_{in} = 1.2\ V) = R_{s_2}(V_{in} = 0\ V) = 43\ \Omega \tag{5.50}$$

The output spectrum for this sizing of S_2 with otherwise ideal components is displayed on figure 5.17.

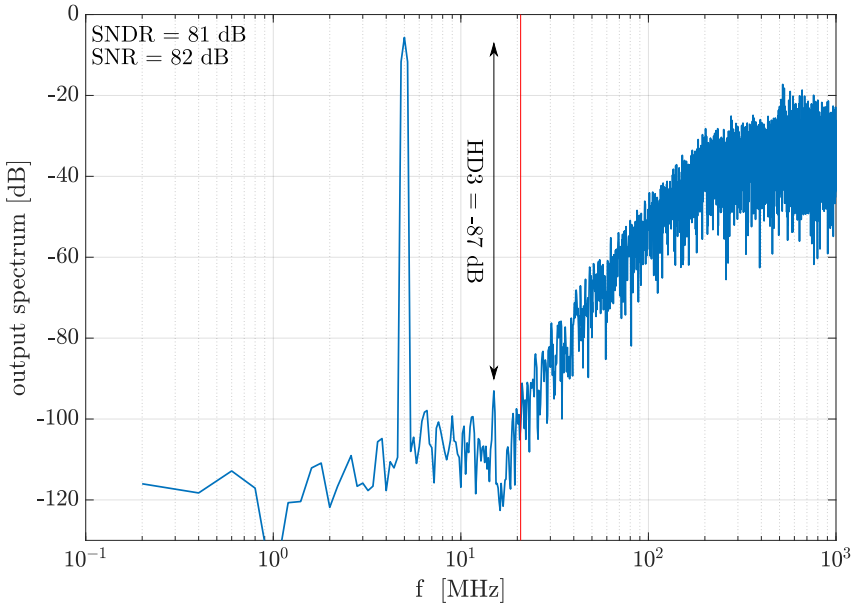


Figure 5.17: Output spectrum of the SDM with third harmonic and 5 MHz input signal of -6 $dBFs$. Bandwidth of the SDM in red.

One possible solution to this problem is using a supply voltage of 1.3 V, which is allowed since

the technology must tolerate a 10% change compared to the nominal supply voltage. This will lead to a lower resistance and non-linearity with no added parasitic capacitance. This method does introduce risks regarding reliability. This results in a small increase in SNDR of 0.3 dB.

5.6.3 DAC and Switch S_1

To charge the capacitor C_s, a DAC switching between the analog reference voltages $V_{ref+} = 1.2\ V$ and $V_{ref-} = 0\ V$ is used. The switch consists of an PMOS transistor to V_{ref+} and an NMOS transistor to V_{ref-}. These transistors must be sized large enough to be able to supply the required current to charge C_s within ϕ_1. Directly connecting the comparator output to the DAC switch would lead to unacceptable delays, so a tapered buffer is used as DAC driver. In order to charge C_s during only ϕ_1, conventional designs would use AND operations of the comparator outputs and ϕ_1 as input of the DAC drivers. However, due to the delay introduced by the DAC driver, this design would cause the DAC switch to be operated during the first part of ϕ_2 and charge C_s and $C_{lp,fb}$. The proposed solution is shown on figure 5.18. The DAC switch itself is driven by the output of the comparator via the DAC driver and followed by a transmission gate that forms a closed switch during ϕ_1. This way C_s and $C_{lp,fb}$ are not charged during ϕ_2. Since the advantages of this technique are limited and it introduces a risk concerning reliability, this was not performed for the final circuit.

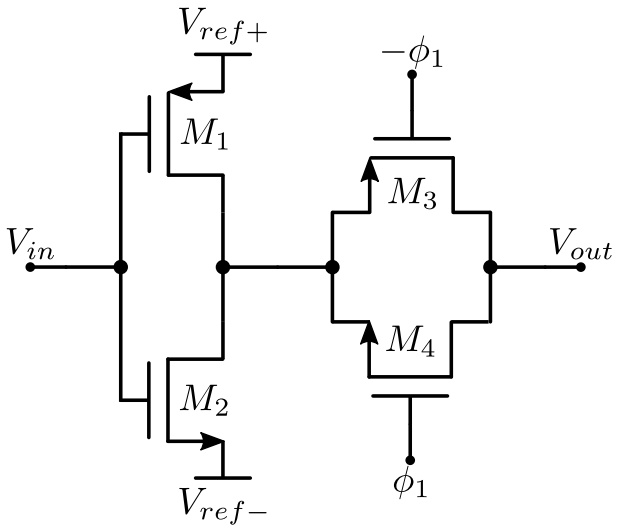


Figure 5.18: Equivalent AND gate.

Redefining the clock phases

C_s is charged during ϕ_1. Unfortunately, during the first part of ϕ_1, the input of the LPSC DAC is still the output that was obtained in the previous clock cycle, since the comparator has either not yet made a decision, or this decision has not yet propagated through the DAC driver to its output. Depending on the previous and the current output, it is possible that C_s will be charged towards the wrong voltage during this period. Due to comparator delay and metastability and the added delay of the DAC driver, this can take quite a while and lead

to an highly increased power consumption. Due to the comparator metastability, C_s was also not always fully charged at the end of ϕ_1. This can be solved by increasing the sizing of the transistors in the DAC charging C_s, but this will worsen the first problem of increased power consumption. These problems can both be solved by exchanging ϕ_1 and ϕ_2 as displayed on figure 5.19. This gives an entire half clock cycle for the comparator to make a decision and this decision to propagate through the DAC driver, making the system immune to the comparator metastability and guaranteeing that when ϕ_1 goes high, the input of figure 5.18 will already be stable and C_s can be charged to the correct voltage right away without additional power consumption. Due to this redefinition of the clock phases, all integrator coefficients must be recalculated, since this means the exponential pulse is delayed with an additional half clock cycle. $P(s)$ is now

$$P(s) = \frac{1 - \gamma e^{-sTs}}{s\tau + 1} \frac{\tau e^{-sT_s}}{R} \tag{5.51}$$

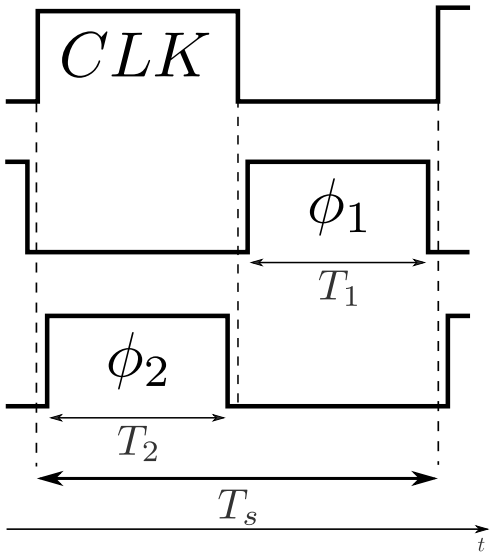


Figure 5.19: New definitions for the clock signals.

Sizing

The transistors M_1 to M_4 will all operate in triode and again introduce a resistance. V_{ref+} and V_{ref-} are constant voltages, which means simple PMOS and NMOS switches can be used for M_1 and M_2 and the resistances of all transistors will be constant. The transistors will be sized to have equal resistance R_{S1} when switched to $V_{ref,+}$ and $V_{ref,-}$. The time constant to charge C_s then becomes

$$\tau = C_s R_{S1} \tag{5.52}$$

The time to charge a capacitor is usually defined as 5τ, but the LPSC DAC is very sensitive to variations in the charge on C_s. To provide some margin, it will be demanded that the voltage on C_s reach within 50 μV of V_{ref+} or V_{ref-} at the end of ϕ_1. This is achieved in 10τ, so R_{S1}

	W [um]	L [nm]	Remarks
M1	60.4	60	
M2	19.3	60	
M3	27.5	60	LVT
M4	9.2	60	LVT

Table 5.5: Sizing for the DAC and S_1

becomes

$$R_{S1} = \frac{250\ ps}{10C_s} = 75\ \Omega \tag{5.53}$$

M_3 and M_4 will sized equally to the transistors in S_2, to guarantee an equal on and off switching behaviour. They are also implemented as low threshold voltage transistors. Since for this sizing $R_{s_2}(V_{in} = 1.2\ V) = R_{s_2}(0\ V) = 43\ \Omega$, this means the triode transistors M_1 and M_2 are allowed to introduce a maximal resistance of 32 Ω. The sizing of table 5.5 is obtained. Charging C_s consumes a lot of power. The power consumption in each DAC is 354 μW, for a total of 708 μW. It is possible to reduce the size of C_s and the power consumption while still meeting thermal noise constraints and obtaining the same τ. However, this will lead to a reduced R and consequently an increase in the size of $C_{lp,fb}$, which is already very large. This does lead to a slightly larger robustness of τ against RC time constant variations, since a larger proportion of the resistance will be implemented as switched-capacitor. Another trade-off consists of increasing the allowed thermal noise level and decreasing C_s. Reducing C_s will also reduce the constraints and power consumption of the DAC driver. It was decided to keep the original design due to area and noise concerns.

DAC driver

The DAC driver is a tapered buffer, in which multiple invertor stages are chained to obtain the desired delay, and the width of each stage is β times the width of the previous stage. This is illustrated on figure 5.20. To minimize delays, two variables must be determined: the taper factor β and the number of stages N. The tapered buffer model introduced in [17] is used, which is shown on figure 5.21. The output capacitance of the n-th invertor in the chain can be split up in an self-loading capacitance $\beta^n C_x$ due to the invertor itself and a load output capacitance $\beta^{n+1} C_y$ due to the next stage. The load output capacitance of the last stage is the load capacitor C_L formed by the DAC transistors. This is illustrated on figure 5.20. The ratio $\frac{C_x}{C_y}$ is technology dependent and also takes into account short-circuit currents. For modern technologies, it can be approximated as 1 [16]. The PMOS transistors will again be sized 3 times larger than the NMOS transistors. Using the equivalent resistance R from equation 5.42, we first define

$$\tau_i = R(C_x + C_y) \tag{5.54}$$

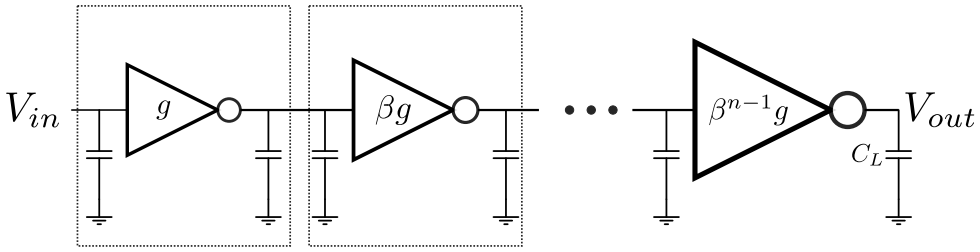


Figure 5.20: Tapered buffer, with $g = \frac{1}{R}$.

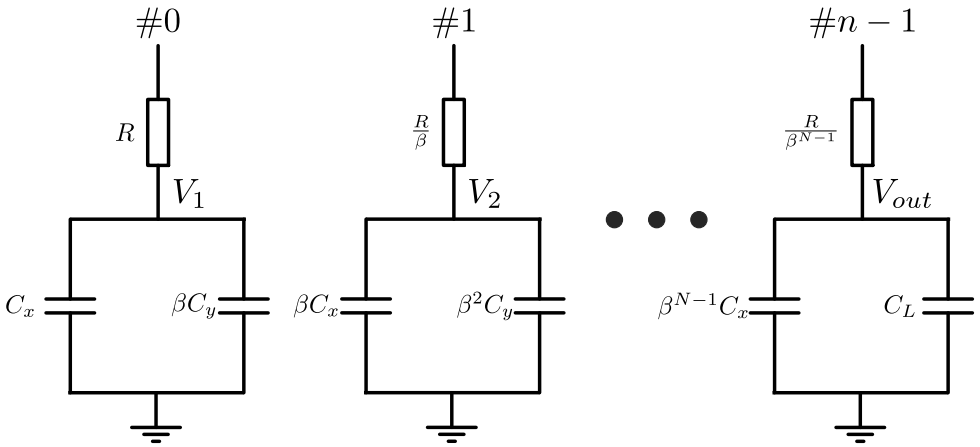


Figure 5.21: Model of the buffer.

The n'th invertor has a time constant τ_n of

$$\tau_n = \frac{\beta^n C_x + \beta^{n+1} C_y}{\beta^n g} = \frac{C_x + C_y + (\beta - 1)C_y}{g} = [1 + (\beta - 1)p]\tau_i \tag{5.55}$$

Where

$$p = \frac{C_y}{C_x + C_y} \tag{5.56}$$

This is independent of n, so the propagation time of the total buffer can simply be determined as

$$t_{tot} \approx ln(2) N \tau_n \tag{5.57}$$

β is also expressed as

$$\beta^N = \frac{C_L}{C_y} \tag{5.58}$$

The first invertor will be minimally sized to reduce the load on the set-reset stage of the comparator. C_L and C_y are then found by simulation as $C_L = 70.5\ pF$ and $C_y = 290\ aF$. As the amount of invertors N increases, so will the power consumption due to an increased total capacitance that needs to be charged, short-circuit currents and leakage currents. To minimize power consumption yet reach an acceptable timing, N is chosen as the smallest amount of stages resulting in a propagation delay lower than 150 ps. This results in

$$N = 3 \ \ \& \ \ \beta = 6.28 \ \ \& \ \ t_{tot} \approx 130\ ps \tag{5.59}$$

Each DAC driver consumes 112.0 μW, for a total of 224.0 μW.

	W [nm]	L [nm]
M7	235	60
M8	120	60

Table 5.6: Sizing for the RTO DAC.

5.7 RTO DAC

The RTO DAC switches between V_{ref+} and V_{ref-} and again consists of an NMOS and PMOS transistor operating in triode. With V_{CM} the common-mode voltage at the input nodes of the third opamp, the magnitude of the current I_{RTODAC} that must flow through each switch is

$$|I_{RTODAC}| = \frac{V_{ref+} - V_{CM}}{R_{3,fb}} = \frac{V_{CM} - V_{ref-}}{R_{3,fb}} = 24\ \mu A \tag{5.60}$$

The constant switch resistance will be taken into account as follows. The switches will be sized as small as possible to reduce delay due gate capacitance. However, the current when switched to V_{ref+} and V_{ref-} must be equal, so the PMOS and NMOS must be sized to obtain an equal triode resistance. Finally, the resistance is quite large with $R_{RTO} = 9.4\ k\Omega$, meaning the magnitude of the delivered current will be smaller than the needed 24 μA. To correct this $R_{3,fb}$ will be tuned again to obtain a satisfactory current.

$$R_{3,fb} = 25\ k\Omega - R_{RTO} = 15.6\ k\Omega \tag{5.61}$$

The RTO DAC is small enough and can immediately be driven by the output of the digital circuitry described in subsection 5.5.3. The sizing for the RTO DAC is shown in table 5.6. Each RTO DAC consumes 8.6 μW, which leads to a total of 17.2 μW. The total power dissipated in $R_{3,fb}$ itself will be double, since half of the time the RTO DAC will sink the current through $R_{3,fb}$.

5.8 Digital chain

All components so far have been largely discussed individually. To provide some overview, a schematic view is presented of the different blocks and how the negative feedback is created on figure 5.22. The left and right sides of each block represent the inputs and outputs, where the + sign refers to V_{in+} or V_{out+} and the - sign to V_{in-} or V_{out-}. As mentioned before, the real circuit is implemented differentially. Differential circuits are usually drawn with a lower and upper path. On figure 5.22, the lower differential path is represented with a - and the upper path with a +. The node just after the signal inversion of the last opamp on figure 5.6 will be called *int*. The inputs of the first and third integrators are called 1 and 3 respectively.

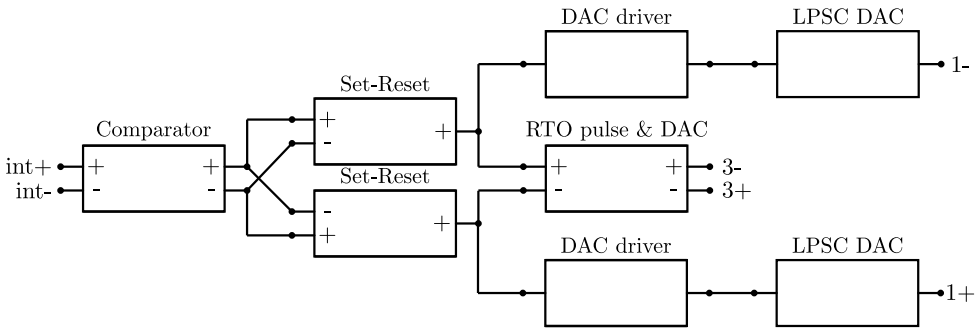


Figure 5.22: Schematic overview of the digital chain.

5.9 Clock generator

The circuit used to generate the clock signals is shown on figure 5.23. It consists of 2 OR gates, each followed by a delaying chain of invertors. Its operation is as follows. Assume CLK makes a transition from 0 V to V_{DD}. In this case, the previous outputs were $\phi_1 = V_{DD}$ and $\phi_2 = 0\ V$. The signal at ϕ_{1d} becomes V_{DD} due to CLK going high. After a delay d, ϕ_1 goes low. Since both ϕ_1 and $-CLK$ are low, the signal at ϕ_{2_d} goes low, finally resulting in a voltage of $\phi_2 = V_{DD}$ after another delay d. This confirms the correct functioning of the clock generator: ϕ_1 goes low before ϕ_2 can go high. The same reasoning is valid for a transition of CLK from V_{DD} to gnd. In this case, the ϕ_2 will transition before ϕ_1 can. We choose $d = 5\ ps$. This was taken into account when calculating the integrator coefficients.

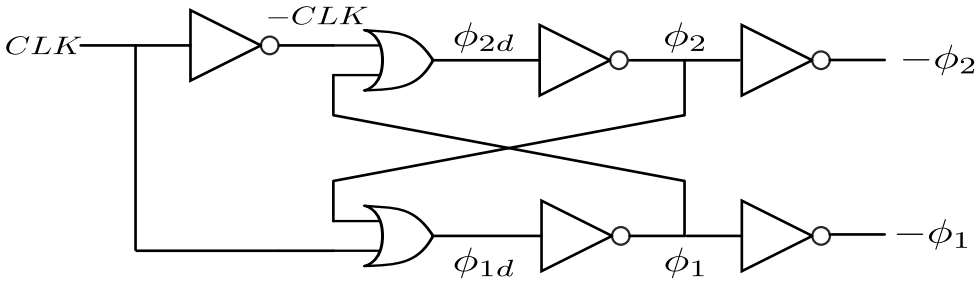


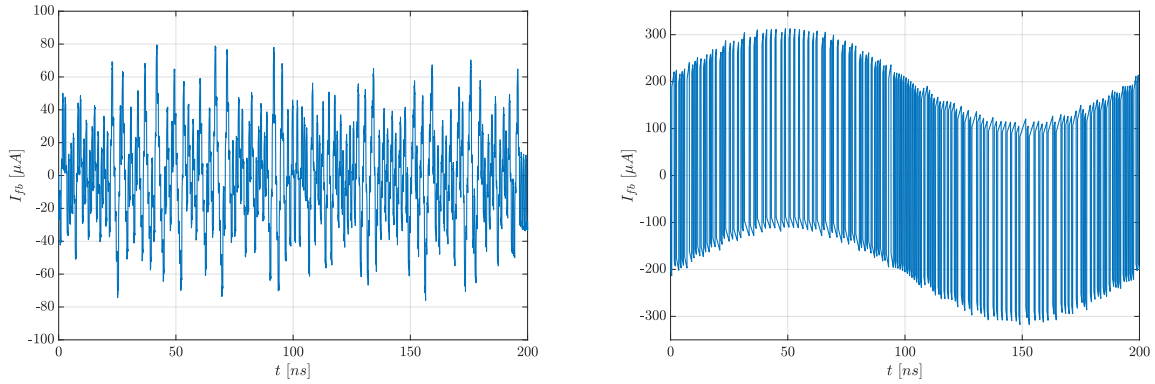
Figure 5.23: Clock generator circuit.

Due to time constraints, the clock generator was not implemented on a transistor level.

5.10 Results

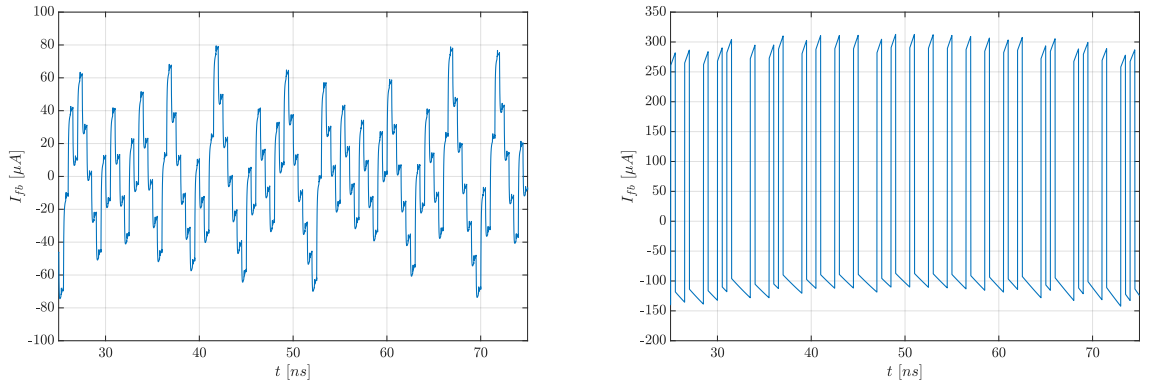
With this finished design, it is now possible to examine the current delivered by the first opamp compared to an ideal reference system using NRZ DACs. The reference system uses the same resistors to make a fair comparison. The current at one of the outputs of the first opamp is plotted for a period of a 5 MHz signal for both the developed as the reference system. This is shown on figure 5.24. On figure 5.25, this is zoomed around 50 ps. The results are dramatic. First of all, the peak currents have been reduced from 312.8 μA for the reference system to

79.12 μA for the designed system with LPSC DAC. It is also clear from 5.25, that the slew rate requirements of the opamp in the designed system will be drastically reduced. The reduced constraints will allow for a much more efficient design of the opamps. As a final benefit, we'll analyse the delivered current. If the current at one output is negative, that means the output sinks current. Due to the differential operation, the other output will deliver the same current. The total mean current delivered by the opamp decreases from 171.2 μA in the reference system to 24.8 μA.



(a) LPSC DAC. **(b)** NRZ DAC.

Figure 5.24: Current at one output of the first opamp for the two systems.



(a) LPSC DAC. **(b)** NRZ DAC.

Figure 5.25: Current at one output of the first opamp for the two systems zoomed in around 50 ns.

The output spectrum for the final circuit is shown on figure 5.26. Due to time concerns and the fact that the operational amplifiers are not yet integrated in the SDM, this simulation does not take into account noise except the quantization noise. An SNR of 82 dB is obtained, which is in line with expectations. However, the HD3 is higher than initially expected based on 5.17. We find $HD3 = -83\ dB$ and as a consequence, the SDNR is lower than expected with $SNDR = 70\ dB$. It is probable that the delay $d = 5\ ps$ in the clock generator circuit is insufficient and the switches S_1 and S_2 slightly overlap when turning on or off.

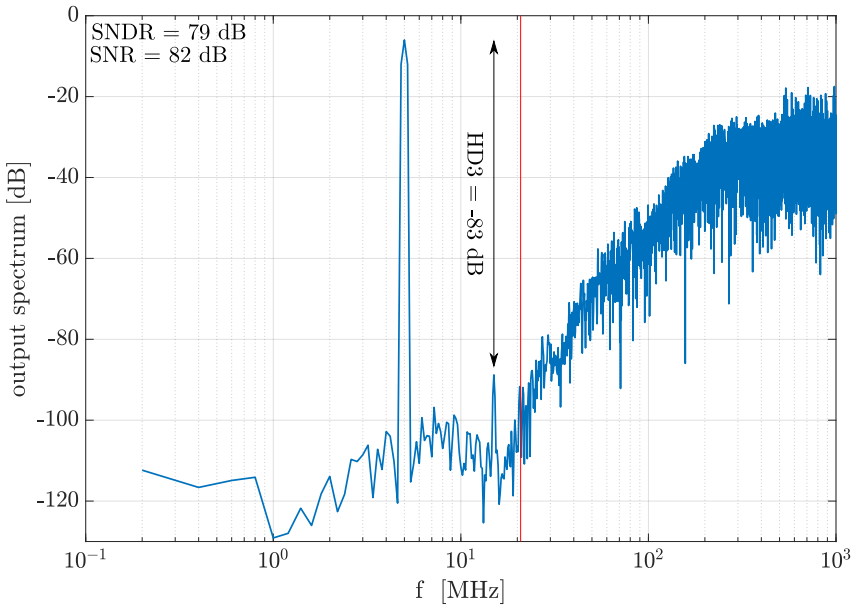


Figure 5.26: Output spectrum of the final circuit for a 5 MHz input signal of -6 $dBFS$. Bandwidth of the SDM in red.

Chapter 6

Conclusion

In this thesis, a SDM was implemented using the LPSC DAC proposed in [1][1]. The sampling rate is 2 GHz with an oversampling rate of 48, resulting in a bandwidth of 20.83 MHz.

In chapter 3, the LPSC DAC was extensively analysed and it was concluded that its transfer function is the product of a DT low-pass filter $H_{lp}(z)$ and a CT decaying exponential pulse $P(s)$. One of its main advantages is its filtering operation, causing high-frequency quantization noise in the feedback path to be filtered out, which strongly reduces the current the first opamp must deliver and relaxes its requirements.

In chapter 4, the LPSC was made transparent by compensating the additional pole by a compensating zero τ_c in the CT loop filter. This way, the NTF could be independently designed of the LPSC. The STF was restored by a pole in the input branch. A system design based on a cascade of integrators with feedforward and feedback was used, with an input feedthrough to the third integrator and local feedback to minimize in-band noise. A Matlab procedure to find the integrator coefficients and compensating zero was developed based on an NTF obtained from the Delta Sigma Toolbox.

In chapter 5, the system was implemented differentially using RC-active integrators. τ was based on thermal noise considerations. While a higher τ lead to more suppression of out-of-band noise, it increased the input-referred thermal noise. τ was sized to result in no more than a 1 dB increase in input-referred noise due to the input and feedback branch. The resistor sizing was also based on thermal noise considerations. The thermal noise at the output was placed 12 dB higher than the quantization noise floor.

One of the main building blocks of the circuit is the comparator. The StrongArm latch was selected for this purpose. Initial implementations of the SDM with an NRZ DAC in the inner path resulted in a large SNR degradation. The cause of this was found to be comparator metastability. To take this into account, the inner DAC was replaced by an RTO DAC, with a fixed feedback pulse and delay. The half-cycle delay provided enough enough time for the

comparator to make a decision. The LPSC switch S_2 was implemented as a transmission gate to allow for a large input voltage range and was optimized for SNDR. To make sure C_s was charged to the right voltage right away, ϕ_1 and ϕ_2 were exchanged.

The circuit was simulated and compared to a reference design using NRZ DACs. The opamp requirements and current delivered by the opamp have been greatly been reduced. The final system has an $SNDR = 79\ dB$ and $SNR = 82\ dB$.

Future work includes a transistor-level design of the clock generator and an analysis of the impact of the non-overlap time between ϕ_1 and ϕ_2 on the HD3. The power consumption of the circuit is currently dominated by the charging of C_s, so further exploring of the associated trade-offs to reduce this power consumption should be performed. Finally, the opamps of the companion thesis should be integrated in the SDM.

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