FACULTY OF ENGINEERING
AND ARCHITECTURE

Design and development of an active [27.5 - 29.5] GHz phased antenna array on-chip with optical beamforming

Hendrik Verhelst
Student number: 01402140

Supervisors: Prof. dr. ir. Sam Lemey, Prof. dr. ir. Bart Kuyken
Counsellors: Prof. dr. ir. Hendrik Rogier, Prof. dr. ir. Guy Torfs, Ir. Olivier Caytan, ing. Quinten Van den Brande, Ir. Laurens Bogaert

Master's dissertation submitted in order to obtain the academic degree of
Master of Science in Electrical Engineering - main subject Communication and Information Technology

Academic year 2019-2020

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Preface

This masters thesis offered me the opportunity to learn new and interesting engineering insights. Therefore, I'm very grateful to my supervisors, prof. Sam Lemey, prof. Bart Kuyken and prof. Guy Torfs, to offer me this opportunity to work on this very interesting topic and share their knowledge on this topic. As this was a multidisciplinary subject, I got in touch with a broad range of fields within the scientific world of electrical engineering, and several research groups of the Department of Information Technology, such as the Electromagnetics and Photonics group and IDlab.

I want to thank my councilors dr. ir. Olivier Caytan, ing. Quinten Van den Brande and ir. Laurens Bogaert as well. They helped me a lot during this research with their knowledge and insights. As well with providing a lot of feedback on my work and teaching me more about processing in the clean room. They impressed me everyday with their knowledge about their research field.

As this master thesis concludes my studies in electrical engineering at Ghent University I want to thank all the professors, assistants and other people at Ghent University to provide me knowledge during courses, projects and exams. Especially I want to thank my two fellow engineering students and best friends, Tim Bomberna and Joppe Massant to help me through these studies. They helped me a lot with feedback and studying, as well as creating a enjoyable time outside the courses.

I also want to thank my family. My mom Isabelle and dad Stefaan for always believing in me and offering me the chance to pursue my dreams. They always supported me in everything I did or want to do. My two brothers, Karel and Willem, for offering a lot of good times at home. At last, I want to thank my girlfriend Kimberly. She has always supported me during these last months, even when I was under a lot of pressure. She is my biggest support and always will be there for me.

Hendrik Verhelst, May 2020

Admission to Loan

Hendrik Verhelst, May 2020

Preamble

Due to the COVID-19 outbreak in 2020, this thesis couldn't be performed as originally planned. The measures taken to limit the further spread of the coronavirus COVID-19 prevented the fabrication and validation of the proposed active on-chip phased antenna array with optical beamforming. While the manufacturing process and the measurement setup are explained in full detail, the validation of the prototype is replaced by a thorough corner analysis to (1) fully understand the effects of manufacturing tolerances that are considered relevant for the topology and to (2) assess the sensitivity of our design. This preamble was drawn up in mutual consultation between the student and the promotors, and was approved by all parties

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Faculty of Engineering and Architecture
Ghent University

Department of Information Technology
Chairman: Prof. dr. ir. Bart DHOEDT

Summary

An active on-chip opto-electronic mmWave phased antenna array with optical beamforming is presented for next-generation mobile communication. First, the used photoreceiver that offers the opto-electronic conversion and amplification is studied. Secondly, an antenna element is designed which adopts an air-filled cavity-backed stacked patch antenna topology and is implemented on a silicon substrate. In the frequency range of interest, ranging from 27.5 GHz to 29.5 GHz, simulation of the antenna element predicts a realized gain of 6.83 dBi, an impedance bandwidth of 3.61 GHz , a total efficiency of 92.6% and a FTBR of 15.7 dB. Furthermore, a 3-dB angular beamwidth of 79.9° in the E-plane and 87.1° in the H-plane are realized. Finally, this antenna element is integrated with the photoreceiver and deployed in a 1-by-4 linear antenna array. The antenna array has a simulated bandwidth of 3.33 GHz, a broadside realized gain of 12.4 dBi and a 3-dB beamwidth in the H-plane of 24°. The grating lobe-free scan range of the antenna array is -40° to 40°. In this range the relative side lobe level stays below -10 dB. A true time delay optical beam forming network is attached to the antenna array to enable squint-free beam steering.

Keywords

5G, millimeter-wave (mmWave), air-filled cavity-backed stacked patch antenna, on-chip antenna (AoC), active photoreceiver, opto-electronic antenna, phased antenna array (PAA), beam steering, true time delay (TTD)

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Abstract- **An active on-chip opto-electronic mmWave phased antenna array with optical beamforming is presented for next-generation mobile communication. First, the used photoreceiver that offers the opto-electronic conversion and amplification is studied. Secondly, an antenna element is designed which adopts an air-filled cavity-backed stacked patch antenna topology and is implemented on a silicon substrate. In the frequency range of interest, ranging from 27.5 GHz to 29.5 GHz, simulation of the antenna element predicts a realized gain of 6.83 dBi, an impedance bandwidth of 3.61 GHz , a total efficiency of 92.6% and a FTBR of 15.7 dB. Furthermore, a 3-dB angular beamwidth of 79.9° in the E-plane and 87.1° in the H-plane are realized. Finally, this antenna element is integrated with the photoreceiver and deployed in a 1-by-4 linear antenna array. The antenna array has a simulated bandwidth of 3.33 GHz, a broadside realized gain of 12.4 dBi and a 3-dB beamwidth in the H-plane of 24°. The grating lobe-free scan range of the antenna array is -40° to 40°. In this range the relative side lobe level stays below -10 dB. A true time delay optical beam forming network is attached to the antenna array to enable squint-free beam steering.**

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I. INTRODUCTION

With the advent of Industry 4.0, the Internet of Things (IoT), smart cities, augmented reality (AR), car connectivity, and other innovative applications, the whole world becomes more and more interconnected [1]. In order to satisfy the diverse and strict requirements set by these applications in terms of data rate, capacity, latency and reliability, the development of the 5th generation of mobile networks (5G) becomes inevitable.

Existing technologies will be pushed to their limits to offer these requirements. In addition, disruptive technologies are investigated and developed to achieve these performance requirements [2]. A first disruptive technology is the utilization of the millimeter-wave (mmWave) spectrum. This spectrum is located from 24 GHz to 300 GHz. Recently several bands were allocated to 5G systems, such as the 26 GHz, 28 GHz and 39 GHz band, which will be vital to support the increase in throughput and capacity. A second evolution for 5G networks, is the switch to high density small-cell architectures. By limiting the number of users per cell, a higher bandwidth per user is available. This goes hand in hand with the adoption of the mmWave spectrum, as the propagation loss is much higher and outdoor-to-indoor penetration becomes more challenging. A third disruptive technology is the use of massive multiple-input, multiple-output (MIMO) antenna systems. Here, base stations are equipped with a large number of antennas, much more than the number of user terminals. This enhances system capacity by applying spatial multiplexing. Finally, by utilizing phased antenna arrays (PAA) beamforming can be enabled at the base stations. This will help to overcome the strong attenuation at mmWave [3], as this beamforming enhances the antenna array gain in a narrow beam pointing in the desired direction.

To enable all these technologies, microwave photonics can be helpful, as this engineering field utilizes the excellent properties of optical fiber, such as low signal loss, high bandwidth and immunity to electromagnetic interference, to improve the performance of wireless systems [4]. Photonics also offers an advantageous solution to beamforming when compared with their electronic counterparts which suffer from low bandwidth, high loss and smaller scanning angles. By deploying true time delay (TTD) squint-free beam steering can be achieved [5].

In this work, an active opto-electronic on-chip transmit phased antenna array is presented for operation in the [27.5 – 29.5] GHz frequency band. This antenna array is configured in a 1-by-4 uniform linear array (ULA) and consists out a hybrid PCB/Antenna-on-chip (AoC) single antenna element. The active opto-electronic conversion is enabled by a photoreceiver containing a photodetector (PD) and low noise amplifier (LNA). A true time delay optical beam forming network is attached to the antenna array to enable squint-free beam steering. This optically fed antenna system can be deployed in an analog radio-over-fiber (ARoF) communication link.

As this antenna is designed to operate at mmWave frequencies, its dimensions are very small. By designing the antenna array as AoC system, standard complementary metal–oxide–semiconductor (CMOS) fabrication techniques can be used, which offer high accuracy up to 1 µm [6]. Several AoC arrays as well as antenna arrays integrated on PCB have been reported in literature, based on different antenna element topologies, such as patch antennas [7][8][9][10], slot antennas [11][12][13], horn antennas [14] and loop antennas [15]. In this work, the compact and highly-efficient air-filled cavity-backed

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stacked patch antenna topology, proposed in [16] is adopted as antenna element for the array.

This paper is subdivided in multiple sections. Section II gives an overall view of the system architecture. In section III, the photoreceiver is discussed briefly. Section IV discusses the design of the antenna array, by first elaborating on the single antenna element and then on the antenna array itself. In section V, measurements are discussed and a sensitivity analysis is conducted. Finally, a conclusion is given in Section VI.

II. SYSTEM ARCHITECTURE

The total system consists of two main parts, being an optical beam forming network (OBFN) and an antenna array.

The OBFN is responsible for applying beam steering, using TTD. By doing so beam squint is avoided, as this technique applies time delay between the antenna input signals instead of a phase delay. The used OBFN is implemented in a photonic integrated circuit (PIC) and is designed at Ghent University. It consists of four optical TTD lines, which are each controlled by 5 thermal switches. The maximal relative time delay ΔT_{max} is 49.6 ps, and can be tuned with a resolution of 1.6 ps.

These two parameters set a limit on the achievable scanning range of the antenna array. For an ULA of N elements, with a uniform spacing of a, the maximal scan angle θ_{max} is given by:

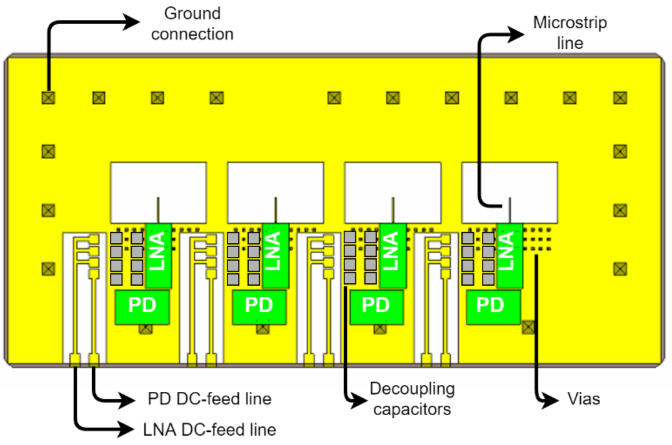
$$\theta_{max} = \sin^{-1}\left(\frac{\Delta T_{max} c}{(N-1)a}\right), \quad (1)$$

with c the speed of light in vacuum. For the 1-by-4 antenna array designed here with an interelement distance of $0.6*\lambda_{min} = 6.1$ mm (λ_{min} is the free-space wavelength at 29.5 GHz), this results in a maximal scan range of ±53.37° and a scanning resolution of 4.54°. Nevertheless, this scan range will not be achieved, as grating lobe-free steering will set a stricter limit, as explained in section IV.B.

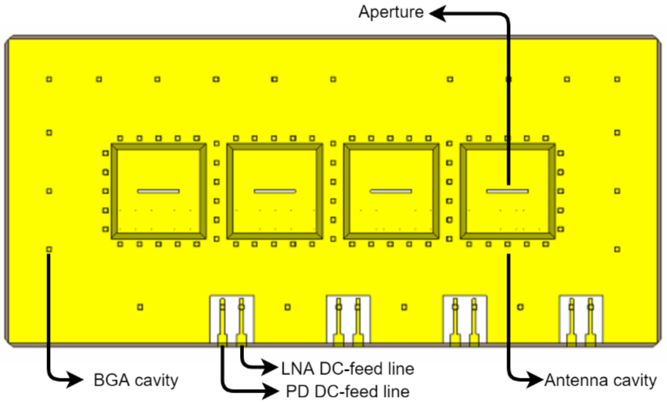
The antenna array itself consist of a silicon (Si) chip and a printed circuit board (PCB). The silicon chip contains the microstrip feed lines, the air-filled antenna cavities and coupling apertures, the photoreceivers, the DC-feed lines for biasing the photoreceivers and feeding the LNAs, and decoupling capacitors (10 nF and 100 nF) to avoid AC signal coupling from the photoreceiver to the DC-feed lines. A schematic representation of the chip is shown in Fig. 1 by a top and bottom view.

The PCB contains the stacked patches and the DC-feed lines. These DC-feed lines are connected to the DC-feed lines on the chip and to a pin-header such that supply voltages for the photoreceivers can be applied. This PCB is used as a rigid carrier for the antenna array as well.

The chip and PCB are attached to each other by using a ball grid array (BGA). By providing a BGA pattern of cavities on both the chip and PCB, alignment can be ensured. BGA balls are placed in these cavities and during a reflow process both components are soldered together.



(a) Top view of the chip



(b) Bottom view of the chip

Fig. 1 Schematic representation of the silicon chip

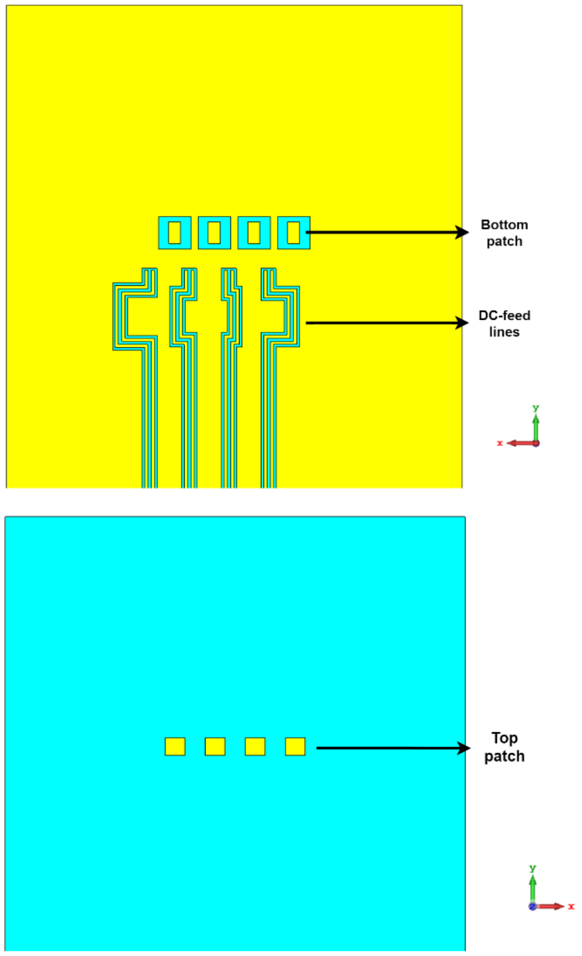


Fig. 2 Schematic representation of the PCB

III. PHOTORECEIVER

The photoreceiver used in this work is designed by Laurens Bogaert and consists of a Ge-on-Si waveguide-integrated vertical p-i-n photodetector (PD) and a GaAs low noise amplifier (LNA) [17], as shown in Fig. 3.The PD converts the incoming optical signal into an electrical current. Then, The LNA converts this current into a voltage and amplifies it. A dedicated LNA design is adopted here to match to the selected PD. These two components are interconnected by wire bonds. The total area of the photoreceiver is 2.943 mm by 5.274 mm.

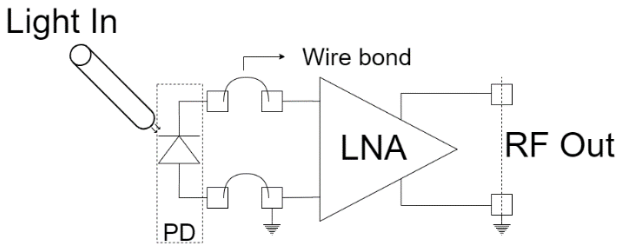


Fig. 3 Schematic representation of the photoreceiver

The performance of the photoreceiver has been validated by measurements. Table 1 is a summary of these measurement results.

Table 1 Measurement results summary of the photoreceiver [17]

Passband , 3-dB [GHz]	Input ref. current noise [pA/√Hz]	Gain	Linearity , OIP3 [dBm]	DC power [mW]
23.5 – 31.5	11.1	S_{21} = 24 dB Z_t =884 Ω	22.2	160 (2V)
	11.3		26.5	303 (3V)

For this work, the output impedance of the photoreceiver is important, as this photoreceiver is interconnected to the antenna array elements. Fig. 4 shows the measured and simulated gain and output reflection coefficient of the photoreceiver, from this last metric the output impedance can be calculated.

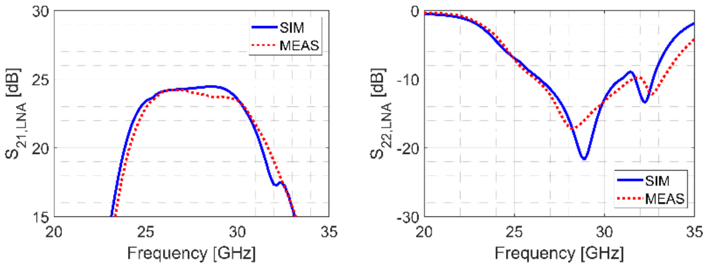


Fig. 4 Gain and output reflection coefficient of the photoreceiver

IV. ANTENNA ARRAY

Development of the antenna array starts with the design of the single antenna element. This is then deployed in an array configuration with the integration of the photoreceiver taken into account.

A. *Single antenna element*

1) *Specifications*

As the single antenna element is the building block of the antenna array, the single element's performance determines to a large degree the final performance of the array. The far-field radiation pattern of the antenna array is the far-field pattern of the single antenna element multiplied by the array factor. So, to have an optimal antenna array performance, the single antenna element should have a wide beamwidth, a front-to-back ratio (FTBR) of at least 10 dB and high gain. Bandwidth should be at least 2 GHz with a center frequency of 28.5 GHz. This translates more specifically in a -10 dB input reflection coefficient in the frequency range of [27.5 - 29.5] GHz. Total efficiency, which includes radiation and mismatch loss, should be at least 90%.

2) *Topology*

The design of the antenna element is based on a hybrid integration strategy for compact, broadband and highly efficient mmWave on-chip antennas designed by Quinten Van den Brande [16]. In this design, a cavity-backed stacked patch antenna is implemented on a 540 µm-thick silicon substrate by means of air-filled substrate-integrated-waveguide (AFSIW) technology. A hybrid approach is adopted in which the antenna feed and air-filled cavity are integrated on chip and the stacked patch configuration is implemented on a high frequency Rogers RO4350B® (ε_r = 3.66 , tan δ = 0.0031) laminate that supports the chip.

The application of two coupled patches results in a significantly increased bandwidth. The air-filled cavity is created in the silicon wafer by using KOH bulk micromachining. This results in skew sidewalls. The electromagnetic fields of the stacked patches reside in this air-filled cavity for the most part, hence surface waves excitation is suppressed and bandwidth and efficiency is increased. Feeding of the patches is realized through aperture coupling from a microstrip on the backside of the silicon substrate. Fig. 6 is a schematic representation of the resulting single antenna element.

3) *Simulation results*

Simulations of the single antenna element predict a -10 dB impedance bandwidth of 3.61 GHz and a total efficiency of 92.6% at 28.5 GHz.

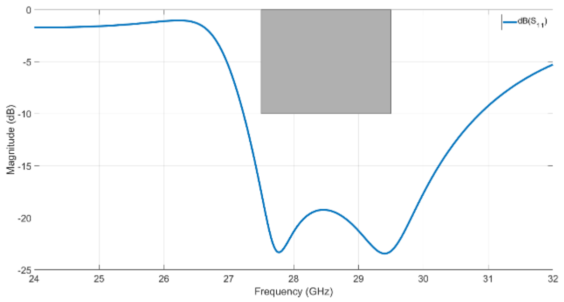
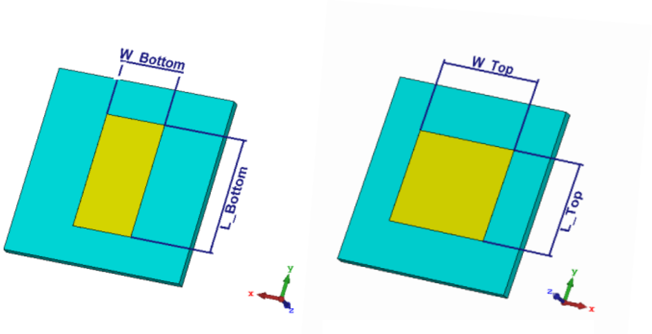
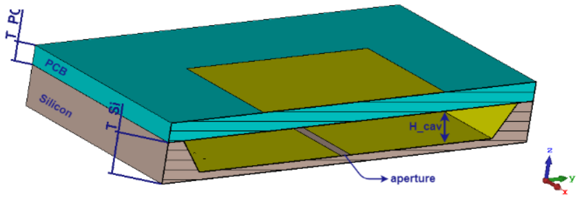


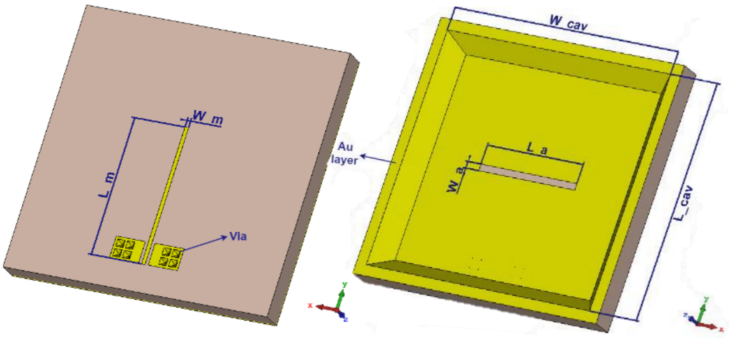
Fig. 5 Simulated input reflection coefficient



(a) PCB top view (b) PCB top view



(c) Cross-section of the single antenna element



(d) Wafer top view (e) Wafer bottom view

Fig. 6 Schematic representation of the single antenna element

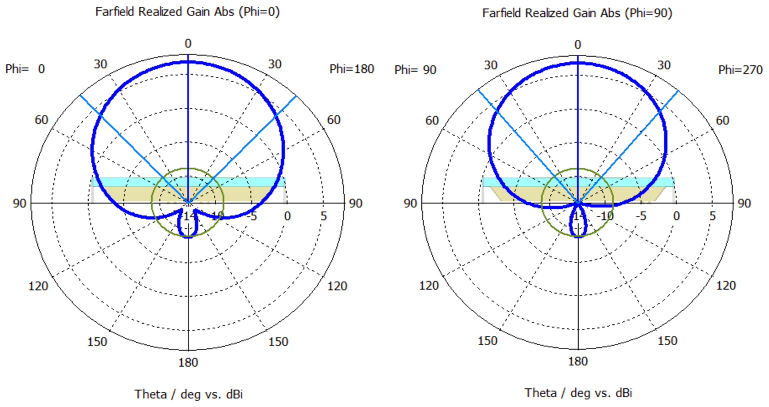


Fig. 7 Simulated radiation pattern

The realized maximum gain is 6.83 dBi in both E-plane (φ = 90°) and H-plane (φ = 0°) and is in the direction of θ = 0°, as shown in Fig. 7. The FTBR is 15.7 dB at 28.5 GHz in both fields. The half-power beamwidth is slightly different in the H- and E-planes, amounting to 87.1° and 79.9°, respectively.

B. *Antenna array*

The resulting antenna element has a total footprint of 5 mm by 5 mm. This is smaller than 0.5 λ_{min} by 0.5 λ_{min}, with λ_{min} the free-space wavelength at 29.5 GHz. This allows for grating lobe-free beam steering of the antenna array.

1) *Topology*

To ensure integration with the photoreceiver, the antenna elements are adjusted to fit these photoreceivers on them. This is done by extending the silicon substrate in the -y direction and shortening the microstrip feed line, by moving the end of the microstrip line closer to the center of the antenna cavity, as shown in Fig. 8. By doing so the bandwidth of the antenna is shifted. Therefore, the coupling aperture size is adjusted to achieve the wanted bandwidth. Integration of a single antenna element and photoreceiver results in a mismatch loss between output impedance of the photoreceiver and input impedance of the antenna, of less than 1 dB in the frequency range [27.5 – 29.5] GHz, as seen in Fig. 9.

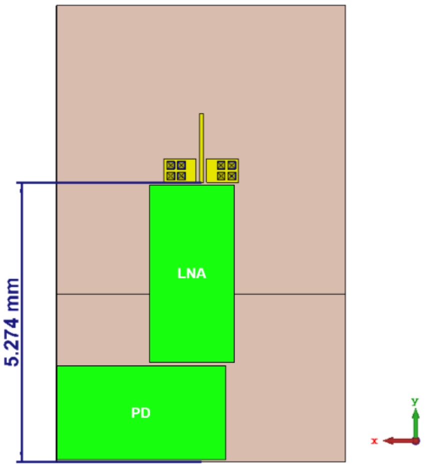


Fig. 8 Photoreceiver placing on the single antenna element

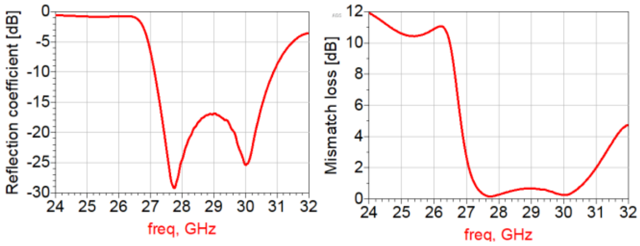


Fig. 9 Mismatch loss between photoreceiver and antenna element

A 1-by-4 configuration is adopted for the antenna array. Due to the integration of the photoreceivers the single element is longer in one direction, as shown in Fig. 8, so lining them up in a 4-by-1 configuration would result in a larger inter-element distance than in the 1-by-4 configuration. This would decrease the maximum achievable scan range due to grating lobes. Grating lobe-free scanning is achieved for a steer angle smaller than:

$$|\theta_{0,max}| = \sin^{-1}(\lambda_{min}/a - 1), \tag{2}$$

The selection of the inter-element distance (a) involves a trade-off between the grating lobe-free scanning range, mutual coupling between antenna elements and structural stability of the antenna. Increasing the inter-element distance results in a decrease in scan range due to grating lobes. But also a decrease in mutual coupling between the elements, therefore the isolation between elements is increased which results in lower losses. A larger antenna is also more robust and stiffer, which makes it easier to handle. For the integration of the PCB and chip ball grid array (BGA) is chosen here. A sufficient inter-

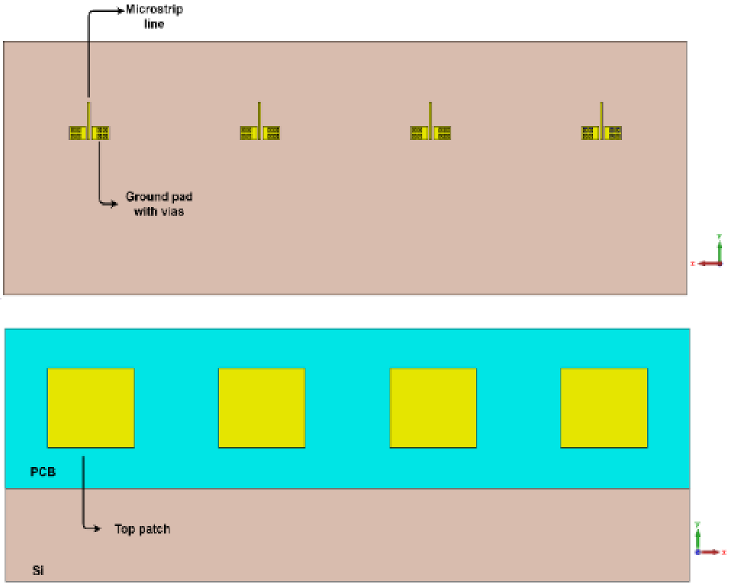


Fig. 10 Top and bottom view antenna array

element distance is needed to place these BGA balls. Therefore, an inter-element distance of 0.6* λ_{min} is chosen here. This results in a grating lobe-free scanning range of ±41.8°, isolation between elements of at least -20 dB. The optimized dimensions are listed in Table 2 and a top and bottom view of the resulting antenna array is shown in Fig. 10.

2) *Assembly and DC network*

By using a BGA to solder the chip to the PCB, an accurate alignment between both components can be achieved due to the self-alignment property of BGA. To this end, small cavities with a volume of half a BGA ball are implemented on the antenna array chip, by means of the same KOH micromachining technique which is used to create the antenna cavities. On the PCB a pattern of solder pads is implemented using a soldermask that matches this BGA pattern.

A DC fed network is required to deliver the supply voltages for the photoreceiver attached on the chip. By utilizing the conductivity of the BGA balls, an interconnection between the DC-feedlines on the PCB and the chip can be created. To decouple the DC lines from the AC signal generated by the photoreceiver, decoupling capacitors of 10 nF and 100 nF are placed on the chip.

3) *Simulation results*

Table 2 Antenna array dimensions

Parameter	Value[mm]	Parameter	Value[mm]
L_{top}	2.710	W_{top}	3.080
L_{bottom}	3.350	W_{bottom}	1.800
L_a	2.365	W_a	0.154
L_m	1.301	W_m	0.074
T_{Si}	0.540	T_{PCB}	0.254
L_{cav}	5.000	W_{cav}	5.000
H_{cav}	0.440		
a	6.097	Configuration	1-by-4

Using these dimensions, given in Table 2, simulations are executed to predict the performance of the antenna array. As shown in Fig. 11, from the passive S-parameters a -10 dB bandwidth of 3.33 GHz, ranging from 27.27 GHz to 30.07 GHz is identified. As shown in Fig. 12, the active S-parameters predict that the antenna is matched in the frequency band of interest up to a scan angle of ±40°, resulting in a total efficiency of at least 86% within this scan range.

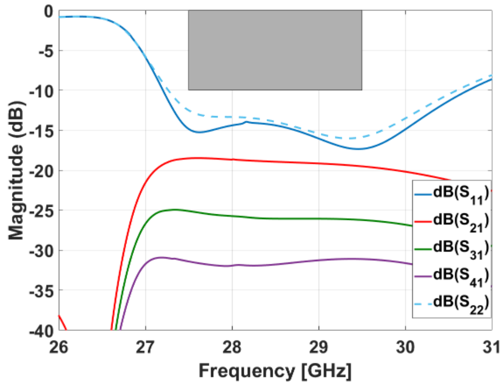
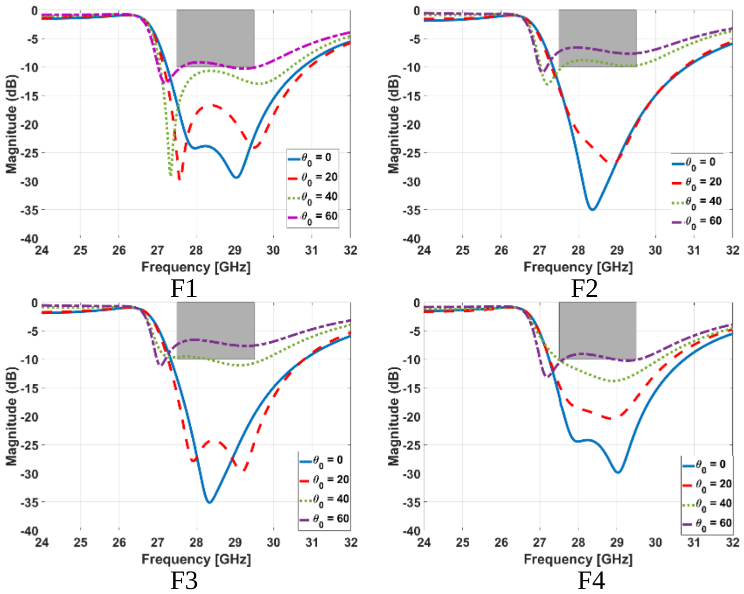


Fig. 11 Passive S-parameters of the antenna array



F1

F2

F3

F4

Fig. 12 F-parameters of the antenna array

The radiation pattern of the antenna array achieves, when the main beam is steered broadside, a realized gain of 12.4 dBi with a relative side-lobe level of -11.9 dB. The gain drops by 3.46 dB and the relative side-lobe level increases to 0 dB when steering at 60°. From the relative side-lobe level, it can be concluded that grating lobe-free steering is achieved up to 40°, as this stays below -10 dB up to this angle. In this range the gain only drops 0.7 dB. The obtained beamwidth of the array is about 24° in the H-plane for all steering angles. As a summary of the radiation performance of the antenna array at 28.5 GHz, Fig. 13a provides the HPBW as a function of steering angle, while Fig.13b shows the realized gain and relative side lobe level as a function of steering angle.

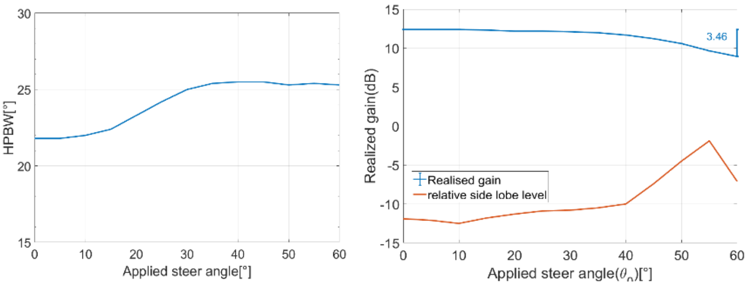


Fig. 13 Summarized far-field pattern of the antenna array at 28.5 GHz

4) *Fiber pigtailing*

A Plexiglass mount is also fabricated. This mount can be attached to the PCB by M1 screws. This mount facilitates the coupling of the input optical fibers to the photoreceiver by mechanically supporting the attached fibers. These fibers should land on the photoreceivers at an angle of 4° to achieve optimal coupling. Note that these screw heads could have an influence on the radiation of the antenna array as they are close to the top patches.

V. MEASUREMENTS AND SENSITIVITY ANALYSIS

Due to the Covid-19 outbreak (see preamble) no prototyping and validation of the antenna array could be performed. The measurement setup is described in a descriptive manner how they would be performed. The discussion of the results of the measurements are substituted for a sensitivity analysis.

A. *Measurement Setup*

The measurements could be performed in an anechoic room. The measurement setup is schematically represented in Fig. 14. Outside the room the output port of a vector network analyzer (VNA) is used to modulate an optical signal. This optical signal is generated by a laser and passes through a polarization controller (PC). To modulate the optical signal a quadrature-biased Mach-Zehnder modulator (MZM) is used. The power of the modulated signal is controlled by a cascade of an erbium-doped fiber amplifier (EDFA) and a variable optical attenuator (VOA) and passes through a PC. This signal is routed to the inside of the anechoic chamber using standard single mode fiber (SSMF). The fiber couples the input signal to the OBFN. The desired time delay is controlled by 20 voltage inputs. The OBFN is connected to the antenna array by 4 optical fibers. These 4 fibers pass through a tunable delay line (TDL) to calibrate out the possible difference in fiber length. The needed bias voltages for the photoreceiver are applied to the antenna array as well. The antenna array is mounted on a positioning system, to be able to characterize the far-field pattern. In the far-field of the antenna array, a standard gain horn receives the transmitted signal of the antenna array. The output of the horn antenna is attached to the input port of the VNA. To validate the antenna array, separate of the OBFN, this last component can be switched to an optical 1-to-4 splitter, drawback of this is that no beam steering can be performed. Using the gain comparison method the radiation pattern of the antenna array can be evaluated.

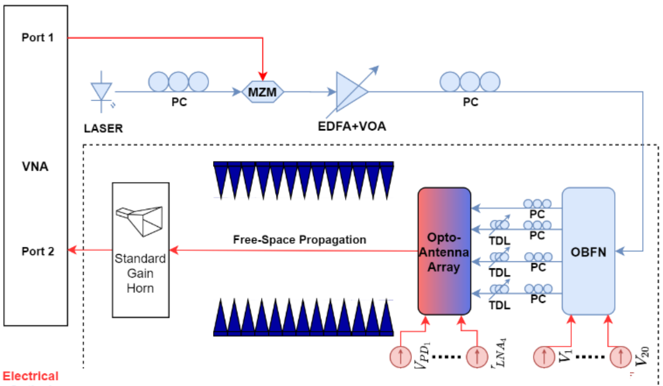


Fig. 14 Schematic representation of the measurement setup

B. *Sensitivity analysis*

In the analysis, several fabrication errors that can occur are simulated to check their influence on the input reflection coefficient of the antenna array. These errors can occur during fabrication of the PCB, silicon chip or their assembly.

Only the fabrication errors with the most influence are discussed here and only the passive input reflection coefficient of the first antenna element is considered, as the other elements shows similar reflections. First, the PCB fabrication tolerance is simulated by displacing the stacked patches simultaneously or separately and by increasing and decreasing the patch size.

Secondly, CMOS fabrication tolerance is simulated by displacing and increasing or decreasing the size of the coupling aperture and microstrip line.

Thirdly, fabrication errors that can occur during bonding of the PCB and silicon chip are investigated. These include a displacement of the chip, which is identical to a displacement of the stacked patches, a rotation of the chip with reference to the PCB, and a height difference between chip and PCB due to the height of the BGA balls.

From the sensitivity analysis it is concluded that the fabrication tolerances during PCB manufacturing and during bonding of the PCB and chip have the most influence. More specifically the input impedance bandwidth of the antenna array changes significant if the patch sizes are increased or decreased, if the patches are misaligned resulting in a y-direction displacement or when the height between PCB and chip is changed. Shown in Fig. 15, Fig. 16 and Fig. 17, respectively.

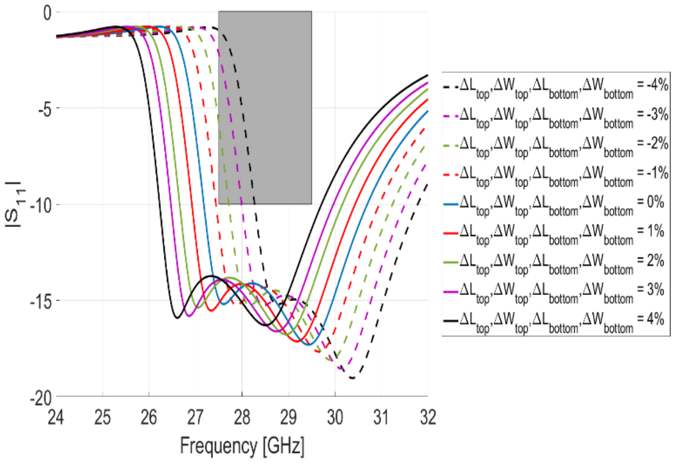


Fig. 15 Input reflection coefficient when the patches are changed in size

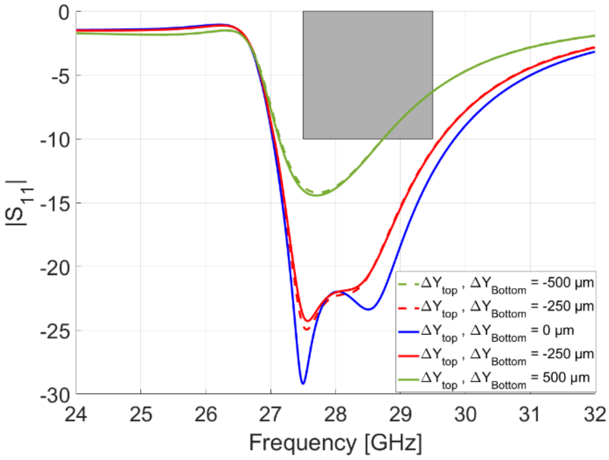


Fig. 16 Input reflection coefficient when the patches are moved in the y-direction simultaneously

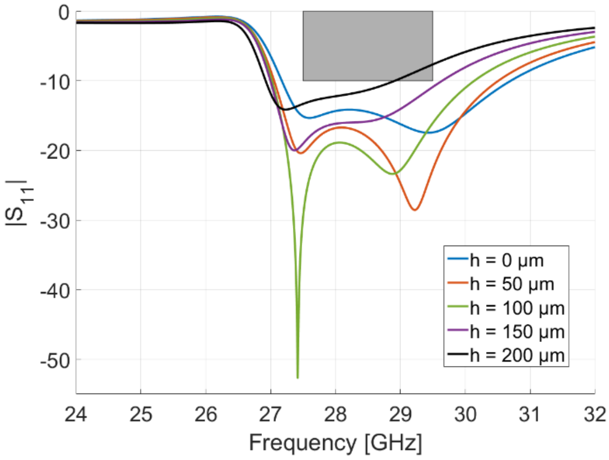


Fig. 17 Input reflection coefficient when height between chip and PCB is changed

VI. Conclusion

In this masters thesis, an active mmWave opto-electronic on-chip antenna array with optical beamforming is developed. The single antenna element follows a hybrid integration strategy for compact, broadband and highly efficient mmWave on-chip antennas which results in an air-filled cavity-backed stacked patch antenna. An 1-by-4 linear array is formed with this antenna element and optimized for integration of a photoreceiver with each element. Together with a TTD OBFN a total transmit system can be created for squint-free beam steering. The resulting antenna has a realized broadside gain of 12.4 dBi and a relative side lobe level of -11.9 dB. A grating lobe-free scan range of ±40° is achieved. Beamwidth of the antenna array in the H-plane amounts to approximately 24°. A -10 dB bandwidth of 3.33 GHz is achieved, covering the frequency band of interest in the entire considered scan range. In addition, a total efficiency above 86% is realized within the scan range. As no measurements are realized, a description of the measurement setup is provided and a sensitivity analysis is conducted.

Realization and validation of the total system remains future work.

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Contents

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Acronyms

5G 5th generation mobile network. vii, 1–5

ADC analog to digital convertor. 6

AFSIW air-filled substrate-integrated-waveguide. 27, 29

AoC Antenna-on-chip. 5, 6, 26

AR augmented reality. 1, 2

ARoF analog radio over fibre. 6

AWG arbitrary waveform generator. 65

BCB benzocyclobutene. 56, 57, 60, 75, 76

BGA ball grid array. vi, 11, 44, 53–56, 58, 60, 72

CMOS complementary metal–oxide–semiconductor. 5, 53, 69

DAC digital to analog convertor. 4, 6

dBi decibels-isotropic. 5

DRoF digital radio over fibre. 6

EDFA erbium doped fiber amplifier. 63

GSG ground-signal-ground. 30

HF hydrogen fluoride. 59

HPBW half power beam width. 26

IFoF intermediate frequency over fibre. 6

IoT Internet of Things. 1, 2

KOH potassium hydroxide. 29, 59

LNA low noise amplifier. iv, v, 7, 9, 10, 18, 20–24, 29, 33, 53, 60, 61, 63, 73

LTE Long Term Evolution. 2, 3

MIMO multiple-input-multiple-output. 2–4

MMI multi-mode interferometer. 15, 16

mmWave millimeter wavelength. 2–5, 7, 8, 15, 27, 74

MZM Mach-Zehnder modulator. 62, 63, 65

O1dBCP output referred 1-dB compression point. 24

OBFN optical beamforming network. 7–9, 11, 15, 16, 57, 63, 74

OIP3 output referred third order intercept point. 24, 25

ORR optical ring resonator. 7

PC polarization controller. 63

PCB printed circuit board. iv, vi, 8, 9, 11, 12, 22, 27, 28, 47, 53–57, 71, 72

PD photodetector. 7, 9, 18–22, 53, 57, 60, 61, 63, 73

pHEMT Pseudomorphic High Electron Mobility Transistor. 21

PIC photonic integrated chip. 15, 16

RAU remote antenna unit. 6, 7, 63

RFoF radio frequency over fibre. 6, 63

RTO real time oscilloscope. 65

SSMF standard single mode fiber. 63

TDL tunable delay line. 63

TIA transimpedance amplifier. 18, 21

TTD true time delay. 7, 11, 14, 15, 74

ULA uniform linear array. iv, 11, 13, 32

VNA vector network analyzer. 62, 63

VOA variable optical attenuator. 63

Chapter 1

Introduction

With the advent of Industry 4.0, the Internet of Things (IoT), smart cities, augmented reality (AR), car connectivity, and other innovative applications, the whole world becomes more and more interconnected [1]. By 2023, the number of global mobile devices will grow from 8.8 billion in 2018 to 13.1 billion [2]. In order to satisfy the diverse and strict requirements set by these applications in terms of data rate, capacity, latency and reliability, the development of the 5th generation of mobile networks (5G) becomes inevitable.

The following sections in this chapter will elaborate on some important concepts of 5th generation mobile network (5G), the goals and the outline of this thesis.

1.1 Next-generation wireless communication

The International Telecommunication Union (ITU) has published a recommendation that defines how the 5G mobile network should look like and what performance it should offer to play a better role to serve the needs of the networked society [3]. Table 1.1 summarizes the minimal functionality criteria following from an online survey of the GSA (Global mobile Suppliers Association) group [4].

Low latency communication is essential for services that need fast responses of the network, to make quick decisions, such as self-driving cars and Industry 4.0 applications [5]. A large connection density is needed to deploy IoT and smart cities [5]. An increase in capacity and spectral efficiency is needed to accommodate higher bandwidth and faster data transfer. Applications like AR and 4K streaming will require these higher bandwidths [3]. Finally, energy-efficient communication is needed for IoT devices that run on battery power to achieve longer autonomy [6].

Parameter	Value
Latency in the air link	<1ms
End-to-end latency	<10ms
Connection density	100x compared with LTE
Area capacity density	1 Tbit/s/km^2
System spectral efficiency	10bit/s/Hz/cell
Peak throughput (down-link) per connection	10 Gbit/s
Energy efficiency	>90% improvement over LTE

Table 1.1: Minimal functional performance criteria for 5G [4]

1.2 Technological advancements to support 5G

New disruptive technologies are being investigated and developed to achieve the 5G performance criteria (Table 1.1), most importantly: millimeter wavelength (mmWave) technology, massive multiple-input-multiple-output (MIMO), small-cell architectures, ... [7]. Depending on the application, and its requirements, one or more technologies can be used. This thesis is mainly focused on ultra-wide bandwidth and ultra-high capacity.

Current Long Term Evolution (LTE) networks operate mostly in low- and mid-frequency bands of 900, 1800, 2100 and 2400 MHz. While these frequency bands offer good propagation through air and penetration properties, such as a relatively low path loss, sub-6 GHz bands are getting more and more congested. Therefore, systems operating at mmWave frequencies are currently under heavy investigation. Several gigahertz of spectrum have recently been allocated to 5G systems, most importantly in the 26 GHz, 28 GHz and 39 GHz bands, in order to support the massive increase in throughput [8]. A drawback of mmWave is the high attenuation through air, 130 dB at 28.5 GHz compared to 112 dB loss at 3.5 GHz over 100m [9]. High atmospheric attenuation is one of the reasons for this disadvantage [10]. MmWaves also have bad penetration properties through glass and foliage, hence a poor non-line of sight communication [11, 12]. A way to overcome these more challenging propagation conditions is by utilizing beamforming.

To be able to use mmWave frequencies, changes in architecture and equipment are needed. A shift towards a small-cell architecture [13] naturally complements mmWave technology because of the short transmission distance the cell size is already limited. By placing more small-cells over the area to be covered, the number of users per cell is reduced, which enhances system capacity. In addition, small-cell architectures facilitate communication over alternative routes if line-of-sight communication is blocked, as shown in Fig. 1.1.c, enhancing reliability of the system [14].

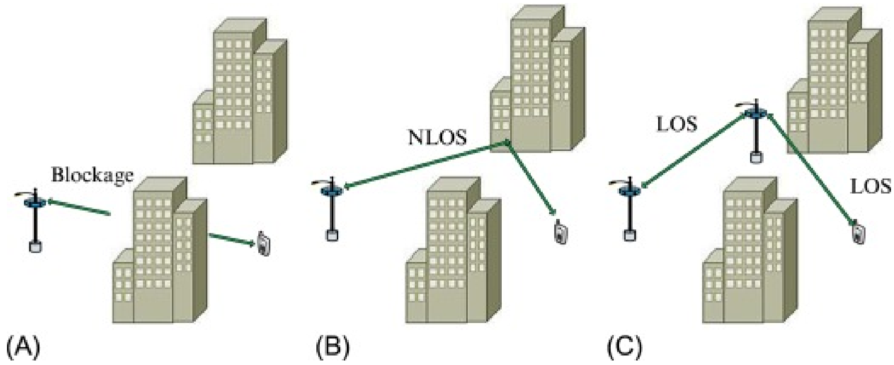


Figure 1.1: How small cell architectures can mitigate non-line of sight propagation conditions. a) Blockage of line of sight by building b) Non-line of sight path by reflection on building c) Alternative route by connecting to an intermediate small-cell base station [14]

A third key technology that will be applied by 5G systems, and which is already in use by LTE, is MIMO communication, where multiple antennas are deployed at the base station and/or the mobile users. This allows to enhance system capacity by applying spatial multiplexing, which exploits multipath propagation to setup multiple spatial data streams using the same time/frequency resources. In 5G this will be pushed further towards massive MIMO, where the number of base station antennas will greatly exceed the number of mobile users [15]. Massive MIMO systems can improve the capacity of wireless communication systems tenfold, compared to multi-user MIMO, by applying massive spatial multiplexing [16]. This can also enhance the energy efficiency by approximately hundredfold, compared to multi-user MIMO [16]. However, this technique entails a larger complexity both in terms of hardware and signal processing. In addition, interference with other base stations and user equipment becomes a greater problem [16].

Due to the use of multiple antennas in massive MIMO, beamforming can be applied to the antenna system. By applying a certain phase difference between the signals applied to the different antenna elements, transmitted energy can be steered into a desired angle due to constructive interference of the radiation patterns of the different antenna elements. This increases the energy efficiency of the antenna system and helps to overcome the challenging propagation conditions of mmWave communication [16]. This can be realized in an analog, digital or hybrid manner. In the analog way each antenna element has a phase-shifter connected to it that applies the needed phase shift, creating one beam. Digital, this phase shift is calculated digital, and applied to the antenna element using a digital to analog convertor (DAC) (and up-converter). Multiple beams are possible, as many as there are antennas. In hybrid beamforming the antennas are connected to a set of phase-shifters. Here, the number of beams is limited to the sets of phase-shifters [16, 17]. While digital beamforming offers great flexibility in number of beams, the hardware cost and power consumption by the DACs is high. Analog and hybrid have a limited number of beams but the hardware cost and power consumption of phase-shifters are lower. The array developed in this thesis can be used in analog or hybrid beamforming. Digital beamforming is also possible if DACs would be integrated as well.

As wavelength scales inversely proportional with frequency, meaning increasing frequency yields short wavelengths. Therefore, antenna footprints will become compacter as well when operating at higher frequencies. The antenna array can be realized using several fabrication technologies. First of all, PCB technology can be used. Here, the radiating elements and other circuit components are integrated on a PCB. Several substrate materials can be used and it can be a cost-effective solution. But on mmWave frequency range, planar circuits and antennas in PCB technology suffer from high losses and are sensitive to increased etching tolerances that could drastically reduce their performance [18]. PCB technology typically has a minimum feature size of around 100 µm [19].

Therefore, the focus of this thesis is shifted towards Antenna-on-chip (AoC) arrays that are compatible with standard complementary metal–oxide–semiconductor (CMOS) fabrication techniques, which offers higher fabrication accuracy, up to 1 µm [20]. The compact antenna footprint, offers an easier and more tightly integration of the antennas and other electronics into one single Si-chip. Unfortunately silicon exhibits adverse properties as an antenna substrate, such as a high relative permittivity ($\epsilon_r = 11.7$) and low resisitivy ($10\,\frac{\Omega}{\mathrm{cm}}$). Hence, applied fields are confined in the substrate and are prevented from radiating freely [21], resulting in a lower radiation efficiency and gain. Table 1.2 summarizes several state-of-the-art antenna arrays with beamforming found in literature, comparing the realized gain (in dBi), bandwidth (in GHz) and maximum achieved steering-angle (in degrees).

For the feeding of the antenna array a choice can be made between electrical or optical techniques. Optical techniques have the advantages of being able to deal with higher RF frequencies, as well as a significantly broader bandwidth, lower losses and immunity to electromagnetic interference compared with their electrical counterpart [30, 31]. Optics can also be extended to the backhaul of 5G communication networks to offer a wired solution where wireless communication is not suited [32].

Especially microwave photonics are used for designing the AoC. Microwave photonics is an engineering field that attempts to exploit the properties of photonic technologies, such as low signal loss, minimal power requirement, high efficiency and bandwidth [33], to improve the performance of wireless systems [34]. One of the most important commercial applications of microwave photonic technology has been the transport and distribution of radio signals over optical fiber [35]. Several signal transportation techniques have been developed.

Ref.	Year	Antenna element type	Freq. [GHz]	Gain [dBi]	BW [GHz]	Max. steer angle [°]
[22]	2016	Microstrip cosecant-squared pattern	10	15.0	3.4	/
[23]	2019	Cavity-backed stacked patch	28	16.5	/	±25
[24]	2019	Folded dual-slot	28	11.3	1.3	/
[25]	2019	Cavity-Backed Slot Antenna	28 & 38	5.6 & 8.8	/	±20
[26]	2019	Patch	28	13.0	3.0	±30
[27]	2019	Horn antenna	28	12.3	2.0	±45
[18]	2015	Cavity antenna in PCB	77	10.0	8.0	/
[28]	2012	Air-dielectric cavity-backed patch antenna	94	13.5	4.6	±25
[29]	2015	SIW magnetic loop AoC	340	7.9	17.0	±48

Table 1.2: State of the art of realized antenna arrays with beamforming

Radio frequency over fibre (RFoF), intermediate frequency over fibre (IFoF), and baseband-over-fiber [34]. The base concept of these techniques is modulating an optical carrier with an electrical signal and transmit it over fiber. In case of RFoF, the input signal is first up-converted to the wanted RF frequency and then used to modulate the optical signal. Baseband-over-fiber works in the opposite way. The input signal is directly used to modulate the optical signal and up-conversion to RF frequency is done at the remote antenna unit (RAU). IFoF is similar to RFoF but the RF signal is first down-converted to a intermediate frequency (IF) before using as modulation for the optical signal, and is back up-converted to RF at the RAU. These three techniques can be implemented analog or digital, termed analog radio over fibre (ARoF) and digital radio over fibre (DRoF). In ARoF all the signals are in the analog domain, while in DRoF the signal that modulates the optical carrier is converted to the digital domain using a analog to digital convertor (ADC) and converted back to the analog domain at the RAU by a DAC [35].

Only analog RFoF is considered in this research, as this minimizes the needed hardware at the

RAU. Only optoelectronic conversion and amplification is needed at the RAU. Disadvantages of this technique is that by operating at high frequencies fiber chromatic dispersion becomes more pronounced and limits the transmission distance [36]. Another disadvantage is the need for high-speed linear optoelectronic devices.

Microwave photonics can also be used to create optical beamforming networks (OBFNs), which provide an integrated solution with excellent properties [37]. With these components squint-free beam steering can be implemented using true time delay (TTD). This technique induces a time delay between different feed signals by using, e.g. optical ring resonators (ORRs) [38]. This is discussed more extensively in Chapter 2.

1.3 Goals and outline

The main goal of this master dissertation is the design, fabrication and validation of an active opto-electronic on-chip mmWave phased antenna array operating in the [27.5 - 29.5] GHz band. The focus is on the array design, fabrication and validation, and the scalable integration of a photo-receiver at each antenna element. The array should achieve a scan angle of [-45, 45] degrees and be as efficiently as possible. As such, four of these arrays can be placed on the vertices of a square to obtain 360° coverage.

This master dissertation is organized as follows. In Chapter 2, the overall system architecture and its components are discussed. In Chapter 3, the photo-receiver is described in detail. The two main parts (the photodetector (PD) and LNA) and measured S-parameters of those components are discussed. Chapter 4 focuses on the antenna array. The single element design and simulation is discussed and the evolution towards the array configuration. The used fabrication technology and techniques are also described. In Chapter 5, measurements are discussed in a descriptive manner, which could not be executed due to COVID-19 outbreak (see preamble for more information). A discussion on the obtained results is substituted by an sensitivity analysis. The final chapter contains a conclusion and provides an outlook for further research.

Chapter 2

System architecture

In this chapter, an overall view is provided on the active mmWave phased array with optical beamforming, latter referred to as the total system. Section 2.1 will discus the total system and its components by making use of a block diagram. Section 2.2 elaborates on how the components are integrated into a chip and PCB. Finally, section 2.3 explains the working and features of the optical beamforming network (OBFN).

2.1 Block diagram

The total system can be divided into three main parts: the OBFN, four photoreceivers and a 1-by-4 antenna array. Figure 2.1 shows the schematic representation of the total system, in a block diagram.

The function of the OBFN is to take the optical input signal and split it into 4 separate optical signals. Second, a time delay is applied to every signal. This time delay is based on the desired steering angle and needed time difference between the input signals of the antenna array to transmit in the direction of this steering angle. This optical beamforming principle will be discussed in section 2.3.

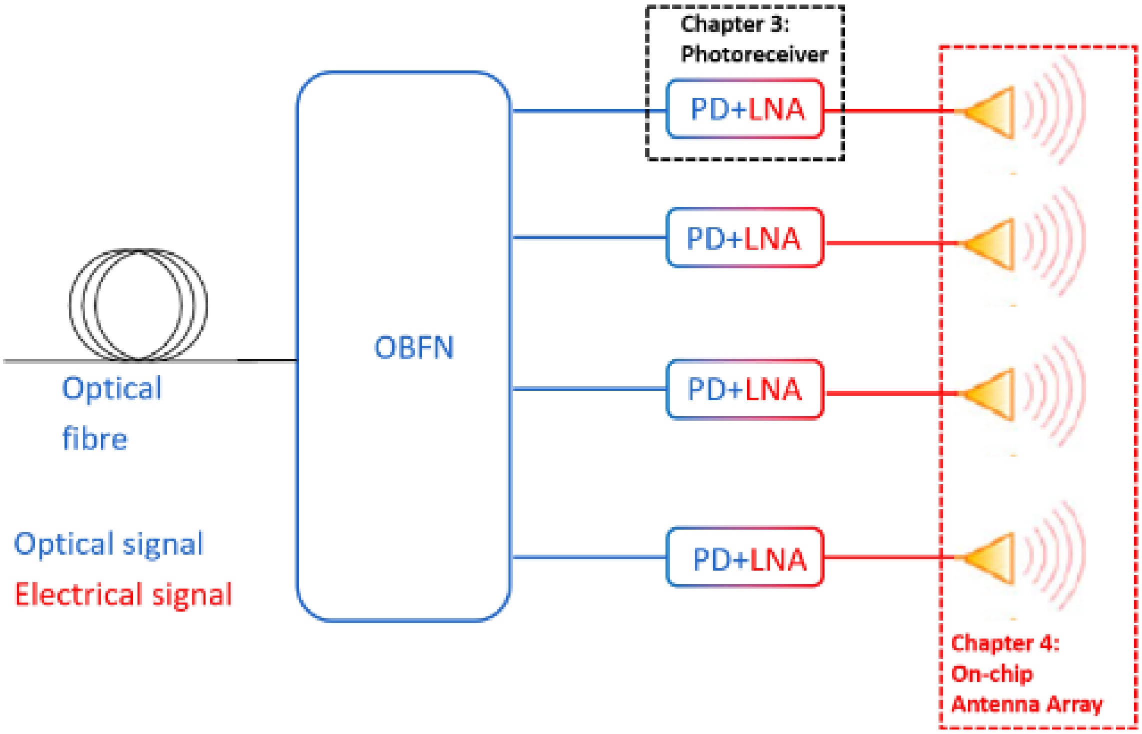


Figure 2.1: Block diagram of the total system

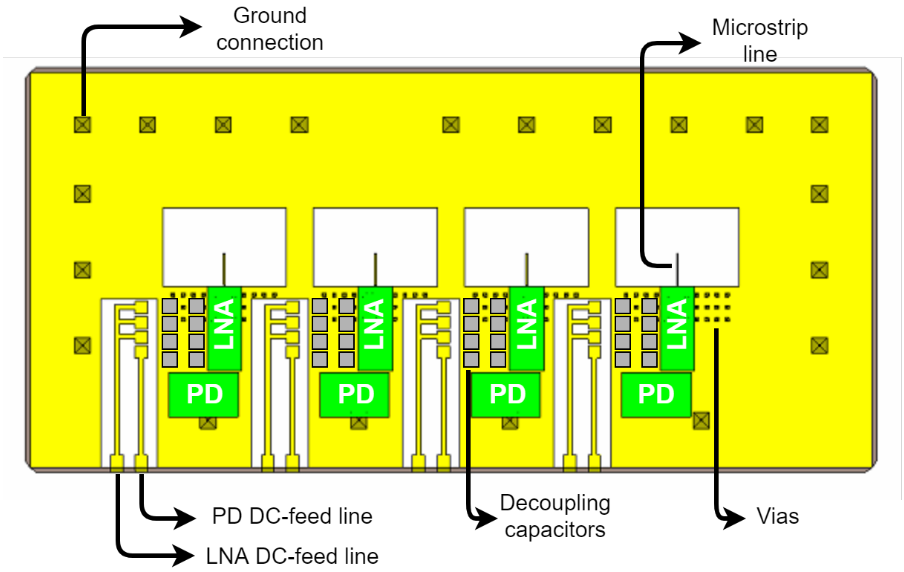
Between the OBFN and the antenna array, a photoreceiver is integrated onto each distinct antenna element. This component transforms the optical signal from the OBFN into an amplified, electrical signal, by making use of a PD and LNA. The complete photoreceiver system is discussed in Chapter 3.

In a final step, the electrical signal is transmitted by an antenna array. The antenna array design is explained in Chapter 4.

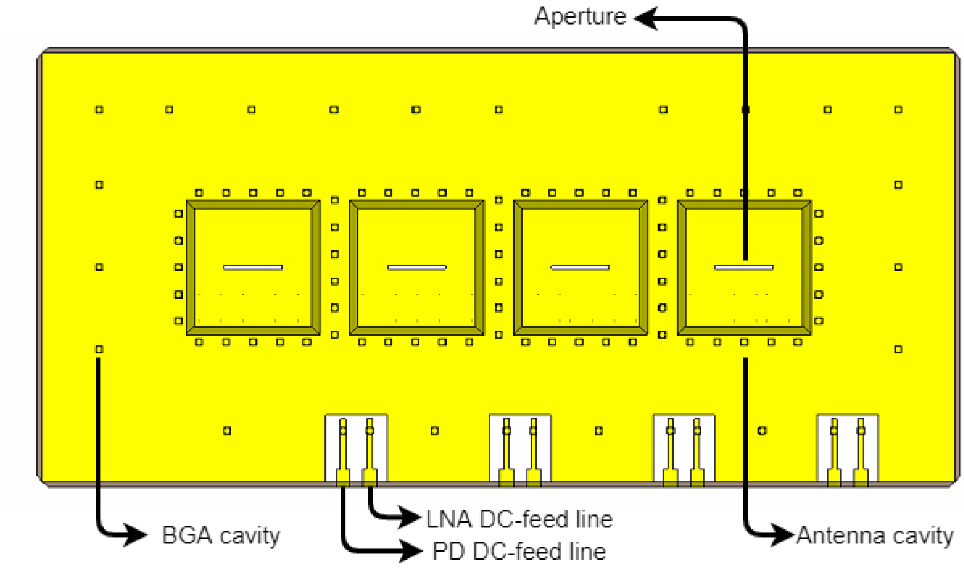
2.2 Integration

In this section, the integration of all components into a single chip and PCB is discussed. This integration can been seen in Fig. 2.2 and 2.3, depicting the top and bottom view of the chip and PCB, respectively.

The antenna array is designed in silicon (Si) and exploits microstrip lines to transmit the signals coming from each separate LNA to each antenna element. The photoreceivers itself are also attached to the array in order to come up with one integrated chip. Next to the photoreceivers, DC-feed lines are integrated as well on the chip.



(a) Top view of the chip



(b) Bottom view of the chip

Figure 2.2: Top and bottom view of the chip

This chip is then attached to a PCB by using BGA balls, this specific technique is elaborated in section 4.3. The function of the PCB is twofold. First, this PCB is used as a rigid carrier for the whole system. Second, it contains the radiating patches and the DC-feed lines to interconnect the photoreceiver, via the on-chip DC-feed lines, to external voltage sources.

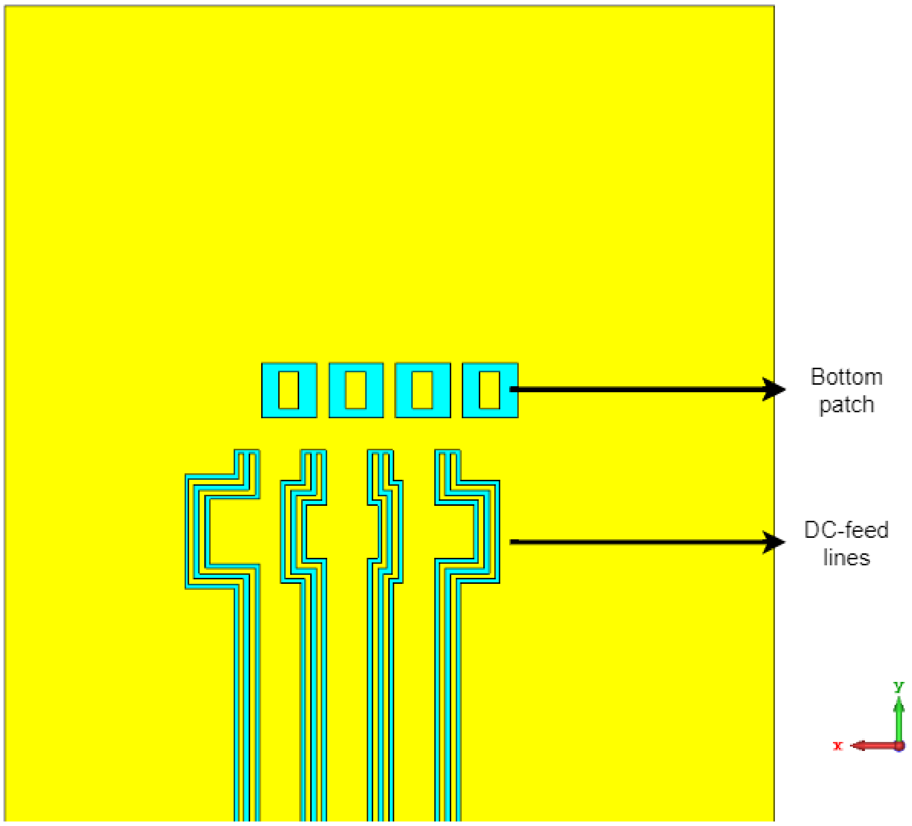
2.3 Optical beamforming network

In this section, the operation of the OBFN is described. First, the general principle of beamforming is explained. Following, the working principle is illustrated specifically by using true time delay (TTD) in an optical way and how this is practically implemented. The latter is referred to as optical beamforming.

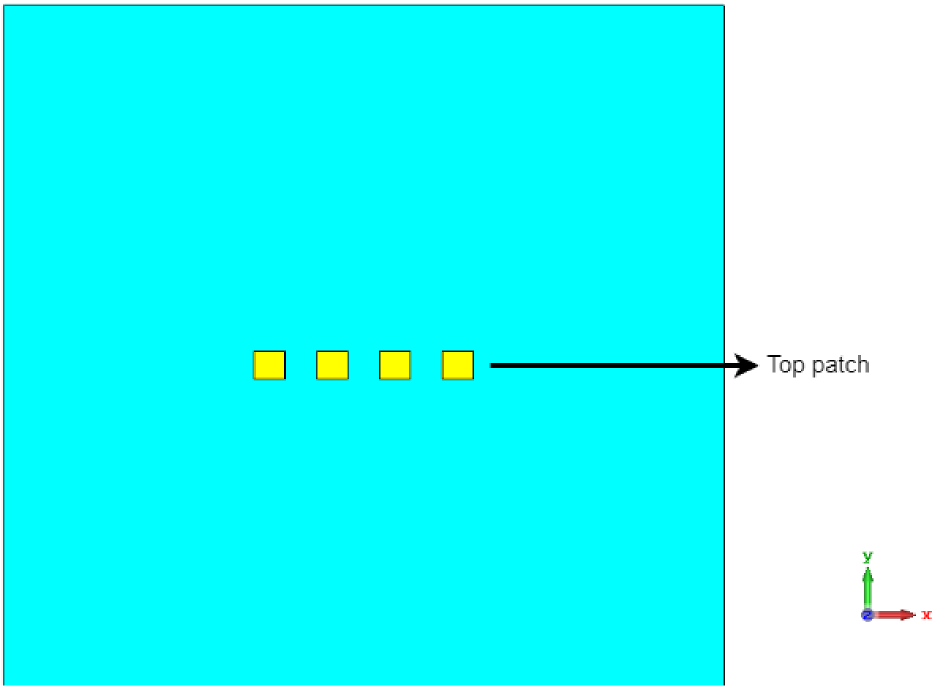
2.3.1 General working principle

By combining multiple antennas into one array configuration, the radiation pattern of this array can be manipulated and an increase in gain can be accomplished. The simplest array geometry configuration consists of N identical antenna elements placed with an equal inter-element distance (a) along a line, say the x-axis (schematic represented in figure 2.4). This array configuration is called an uniform linear array (ULA) configuration. If observation is assumed in the far-field and the radiation vector of each single element $\mathbf{F}(\theta;\phi)$ is assumed identical with no mutual coupling between the antenna elements, then the electric field $\mathbf{e}$ in the far-field of this array can be approximated by [39]:

$$\mathbf{e} \approx \mathbf{F}(\theta;\phi)T(\theta;\phi)\frac{e^{-jk_0R}}{R} \tag{2.1}$$



(a) Top view of the PCB



(b) Bottom view of the PCB

Figure 2.3: Top and bottom view of the PCB

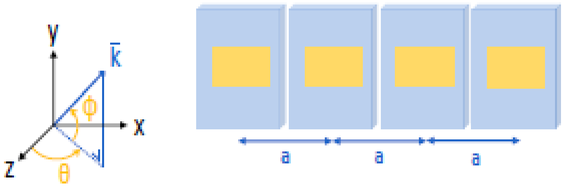


Figure 2.4: Schematic representation of an ULA [40]

a = inter-element distance, θ = elevation angle, ϕ = azimuth angle

With T($\theta;\phi$) called the array factor, calculated by:

$$T(\theta;\phi) = \sum_{n=0}^{N-1} A_n e^{j\beta_n} e^{j\mathbf{k}.\mathbf{s_n}} \tag{2.2}$$

$$= \sum_{n=0}^{N-1} A_n e^{j\beta_n} e^{jnk_0 a cos(\phi) sin(\theta)} \tag{2.3}$$

A_n and β_n are respectively the amplitude and phase of the applied signal to the n^{th} element, $\mathbf{k}$ is the wave vector defined by $k_0\mathbf{u_r} = k_0(cos(\phi)sin(\theta)\mathbf{u_x} + sin(\phi)sin(\theta)\mathbf{u_y} + cos(\theta)\mathbf{u_z})$ and $\mathbf{s_n} = na\mathbf{u_x}$.

To maximize the array factor T($\theta;\phi$) for a certain steering angle (θ_0, $\phi = 0$), beamsteering can be performed by applying a phase delay (β_n) to the antenna input signals. Depending on the desired steer angle θ_0 in the azimuth plane ($\phi = 0$), the appropriate phase delay can be adjusted. For a ULA configuration, beamsteering is achieved by a linearly increasing phase delay given by:

$$\beta_n = -n\delta_0 \tag{2.4}$$

$$= -nk_0 a sin(\theta_0) \tag{2.5}$$

$$= -n2\pi f_0 a sin(\theta_0) \tag{2.6}$$

A_n is kept constant, equal to 1/N, so the maximum of the array factor equals 1. This is to avoid the need for amplitude control on the signals, which would implies extra hardware to perform this need and increasing cost and complexity of the antenna system. The magnitude of the array factor T($\theta;\phi$) in the azimuth plane ($\phi = 0$) is now given by:

$$|T(\theta)| = \frac{sin[\frac{N}{2}(-\delta_0 + k_0 asin(\theta))]}{Nsin[1/2(-\delta_0 + k_0 asin(\theta)]} \tag{2.7}$$

This has a maximum value for a steer angle θ_0 and wave number k_0 ($= 2\pi f_0$). This means that the radiation pattern, defined by equation 2.1, of the antenna array has a maximum in the direction of the steer angle.

In formula 2.5, it can be observed that the phase delay β_n is calculated for the fixed frequency f_0. This steering with constant phase delay may cause problems when steering high-bandwidth signals. When the antenna is excited at other operating frequencies than the frequency f_0 for which the phase delay is calculated, the antenna array will radiate towards an angle different than θ_0. This phenomena is called beam squint [38]. To overcome this, TTD-based beam steering can be used.

2.3.2 True time delay (TTD) vs Phase-shifting

To prevent beam squint, a time delay can be applied instead of a phase delay to the antenna array. This time delay is introduced by exciting each antenna element by a signal that is subject to a linearly increasing time delay (τ_n):

$$\begin{aligned} \tau_n &= -n\tau_0 \qquad (2.8) \\ &= -n\frac{a}{c}sin(\theta_0) \qquad (2.9) \end{aligned}$$

With τ_0 being the time difference between adjacent elements and c the speed of light in vacuum. This TTD τ_n results in a frequency dependent phase difference $\tilde{\beta_n}$ as shown below:

$$\tilde{\beta_n}(\omega) = -\omega\tau_n \tag{2.10}$$

$$= -n\frac{\omega a}{c}sin(\theta_0) = -nkasin(\theta_0) \tag{2.11}$$

As discussed in the introduction, TTD is implemented here by relying on microwave photonics rather than an electronic approach as the latter would result in a big, expensive and complex system operating at mmWave frequencies [38]. The practical implementation is achieved through forming an OBFN.

The OBFN, as described in section 2.1, is implemented in a single photonic integrated chip (PIC) by Laurens Bogaert in the silicon photonics platform imec-ePIXfab SiPhotonics passives [41]. This platform is a fast technology that still requires metallization and heaters to be added in post processing. The total PIC consists of 4 delay arms, each introducing a certain number of discrete time delays (ΔT) between input and output. Fig. 2.5 shows a schematic representation of one delay line.

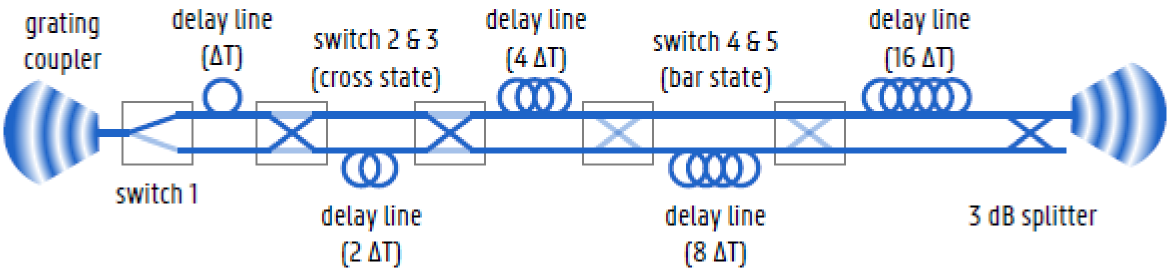


Figure 2.5: Schematic representation of one delay line [40]

Each separate delay arm is build up by using 5 important photonic components, similar to the approach in [40, 42]:

1. A grating coupler. This component is responsible for coupling the input signal from an optical fiber into the delay line. This typically introduces an optical power loss of 6-7 dB.
2. A 3dB splitter. This is a multi-mode interferometer (MMI) configured as a 1-to-2 port splitter. Here, no phase difference between output ports occur.

3. A 2-to-2 port MMI. This is a variant of the MMI but here a $\pi/2$ phase difference between the output port occurs when one of the inputs is excited.
4. A thermal switch. These switches consists out of two 2-to-2 MMIs and two central arms. The phase delay on one of these central arms can be controlled by using resistive heaters. This allows to select at which output either constructive or destructive interference occurs. As such, switches can be tuned into bar state or cross state. In bar state, input 1 is forwarded towards output 1 and equivalently for input 2. In cross state, the inputs get crossed towards the outputs, meaning input 1 goes to output 2 and input 2 to output 1.
5. A two-track delay line. By introducing a path length difference between these two tracks, one of these tracks experiences an extra time delay. equal to $n * \Delta T$.

As seen in figure 2.5, each two-track delay line stage between two switches has an double amount of path length difference. This introduces a doubling of extra delay time. The maximum of delay that can be added to a signal, compared to the time needed to travel along the shortest path, is 31*$\Delta T = 49.6\,\text{ps}$ ($\Delta T = 1.6\,\text{ps}$).

With 5 switches, a 5-bit tunable delay cell is formed. Note that the power levels needed to switch the switches are not identical for every switch. Due to fabrication-induced random phase errors these can differ. But the difference between power levels for cross and bar state are expected to be constant for every switch. To use the PIC discussed here, this would need 20 different voltage supplies, 5 voltages per delay line and there are 4 delay lines. These voltages need to be determined upfront to form a look-up table, to setup the OBFN.

The maximal delay that can be applied sets a limit on the maximum achievable steer angle. Assuming elements are spaced at half-wavelength distance for an operating frequency of 28.5 GHz ($a = \lambda_0/2 = 5.26\,\text{mm}$), the maximum achievable scan angle ranges from -70° to 70°. The given minimal delay, ΔT sets a limit on the scanning resolution. For the same spacing this is 5.2°. Fig. 2.6 shows the relation between relative spacing of the elements and the maximum achievable steer angle and scanning resolution. Based on Fig. 2.6, spacing between the antenna elements result in a trade-off between maximum achievable steer angle and scanning resolution. Furthermore, over-sizing the maximum achievable steer angle with respect to the beamwidth of the antenna array will result in a loss in resolution without improving the maximum achievable steer angle. The spacing between antenna elements has also influence on mutual coupling and grating lobes. This is further discussed in Chapter 4.

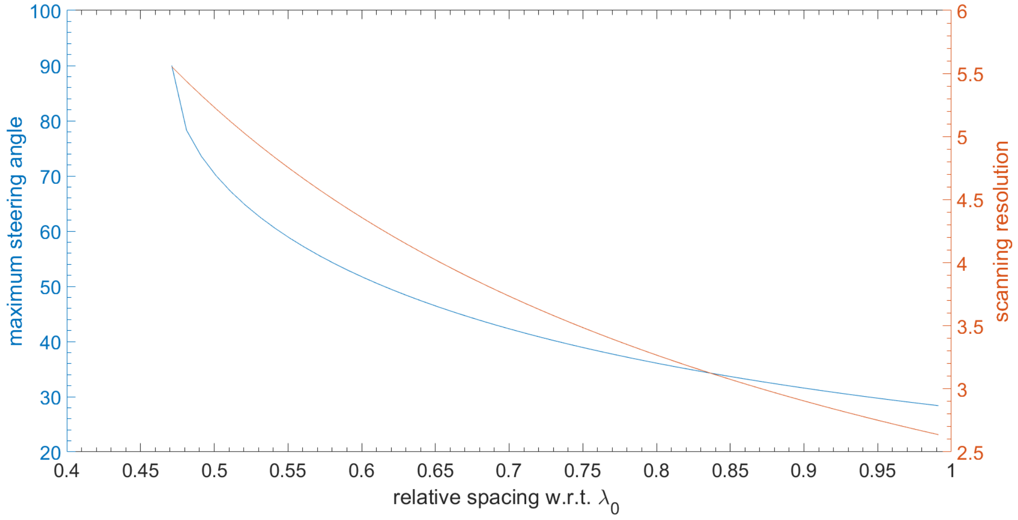


Figure 2.6: Maximum achievable steer angle and scanning resolution as a function of inter-element spacing

Chapter 3

Photoreceiver

In this chapter, the components of the photoreceiver and their operation are discussed more extensively. A photoreceiver has two consecutive functions, namely converting the optical signal into an electrical signal, and amplifying this signal. These functions are performed respectively by a PD for the conversion, and a LNA for amplifying. The components mentioned are more elaborated in section 3.1 and 3.2 respectively.

The photoreceiver used in this research is designed by Laurens Bogaert and is a narrowband photoreceiver, optimized for operating within the [27.5-29.5] GHz band [43]. This photoreceiver consists out of a Ge-on-Si waveguide-integrated vertical *p-i-n* PD and a GaAs LNA. Using a narrowband LNA in the design, rather than a broadband transimpedance amplifier (TIA), allows for a more optimal trade-off between the noise minimization and gain maximization. The resulting photoreceiver is a hybrid system where wire bonding is applied to interconnect the PD and amplifier. Fig. 3.1 is a schematic representation of a photoreceiver, and Fig. 3.2 shows the dimensions and configuration of the photoreiver.

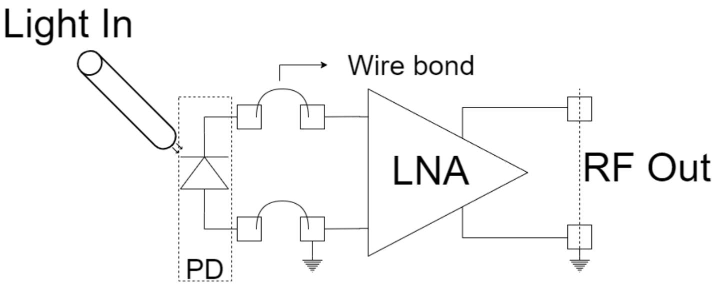


Figure 3.1: Schematic representation of the photoreceiver [43]

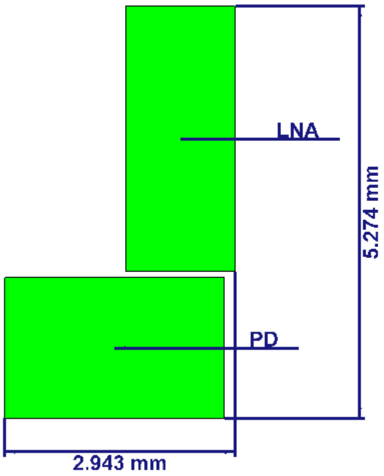


Figure 3.2: Dimensions of the photoreiver

3.1 Photo-detector (PD)

The main objective of a PD is to convert light, made out of photons, to current, made out of electrons. This is achieved by relying on the photo-electric effect of semiconductors [44]. The most basic structure that can be used to form a PD is a p-n junction which consists out of a p-type and n-type doped semiconductor. When a photon strikes the PD with sufficient energy, an electron-hole pair is created. Whether energy is sufficient or not depends on the band gap of the semiconductor used. If this happens within the depletion layer of the junction, the electron and hole will be pulled to the n-type and p-type region respectively due to the built in electric field. This effect is called drift. If the electron-hole pair is created close to the depletion layer, they can diffuse towards the depletion layer before they drift to the n-type and p-type region. In case the PD is reverse biased, the depletion layer is made wider and so the electrons and holes can drift quicker through the PD. The created photo current is proportional to the incident light power. This proportionality is called the responsivity R of a PD and is given by:

$$R = \frac{\text{photo current}}{\text{optical power}} = \frac{\eta q}{h\nu} \approx \frac{\eta \lambda}{1.24} \qquad [\frac{A}{W}] \tag{3.1}$$

With h being Planck's constant, q the electron charge, η the quantum efficiency of the PD, ν the frequency and λ the wavelength (given in µm) of the incoming light.

These specific types of PDs can be modeled as an RC-circuit. With R_s, the series resistance of the PD, arising from the resistance of the contacts. The boundaries of the depletion region act as the plates of a parallel plate capacitor with junction capacitance C_j. This capacitance is directly proportional to the diffused area and inversely proportional to the width of the depletion region [45]. Therefore, the PD operate within a limited bandwidth limited by this RC value.

A solution to decrease this RC value is by decreasing the junction capacitance C_J by increasing the depletion-region width [44]. This can be accomplished by inserting an undoped (or lightly doped) semiconductor layer. As a result, an intrinsic layer is inserted forming a *p-i-n* PD. The optimal width of the intrinsic layer depends on the trade-off between speed and sensitivity. A larger width results in an increased efficiency as more photons can be absorbed, which emerges in a greater responsivity. However, increasing depletion-region width, increases the drift time of the carriers to drift across this region, resulting in a slower device.

In the selected photoreceiver [43], a Ge-on-Si waveguide-integrated vertical *p-i-n* PD is used, which is fabricated using imec's iSiPP50G silicon photonics platform [46]. Responsivity R of this PD is 0.8 A/W at 1550 nm and coupling to the PD is done by using a grating coupler which results in about 5 dB insertion loss. The LNA attached to the PD is designed assuming the reverse bias applied to the PD is 1 V.

3.2 Low noise amplifier (LNA)

An amplifier is needed to amplify the weak current produced by the PD, and to convert it into a voltage [47]. Typically this is done by using a TIA, which is usually a feedback resistor between input and output of an open loop amplifier [48]. These TIAs offer high bandwidth and low noise performances. But such a TIA usually offer gain from DC up to high frequencies with maximal gain flatness over all these frequencies. Using a TIA for narrowband communication requires the TIA to have a bandwidth exceeding the carrier frequency of the narrowband signal while gain is only required in the part of the spectrum where the RF signal is present. This results in a suboptimal solution for wireless communication [49].

Therefore, a dedicated narrowband LNA is designed for the photoreceiver used here [43]. Resulting in an optimal power transfer from the RF signal coming from the PD to the load impedance at the output of the LNA, in the frequency range of interest [27.5 - 29.5] GHz. This design methodology allows for a more optimal trade-off between the minimization of noise and maximization of gain, especially at higher frequencies [50]. Nevertheless, a first drawback of this methodology is that the design is sensitive to the exact values of the parasitics of the PD, i.e. a shifted passband is detrimental due to the resonant nature of the circuit. A second drawback is the need for a dedicated design which depends on the targeted frequency band and adopted PD, and therefore cannot easily be translated to other frequencies or PDs.

The LNA has been designed in a 0.1 µm Pseudomorphic High Electron Mobility Transistor (pHEMT) GaAs technology [51]. As shown in Fig. 3.3, the LNA consists out of three stages. The first stage is responsible for input matching to the PD, taking low noise and high gain into account. Stability is also ensured by placing a parallel RLC network at the output. The input matching network contains a bias tee to enable biasing of the PD and to make sure that the LNA does not get saturated by any DC current generated by the PD.

Design of the second stage is similar to the first one. The main difference concerns the fact that the source impedance follows from the output impedance of the first stage combined with the interstage matching network.

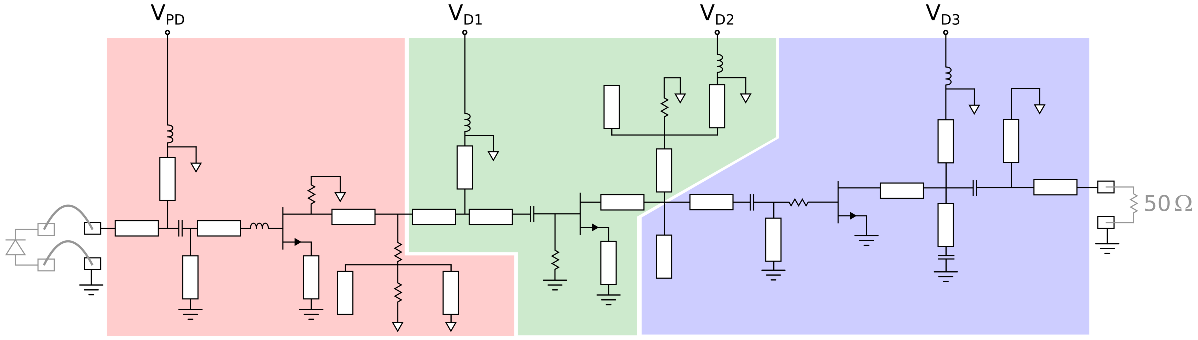


Figure 3.3: Overall schematic of the 3-stage low noise amplifier [43]

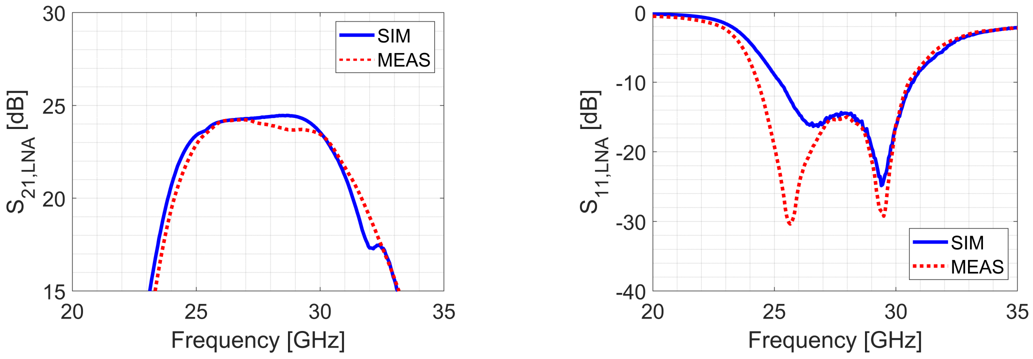
Red: first stage, Green: Second stage, Blue: final stage

The final stage ensures unconditional stability and is matched to a load impedance of 50 Ω.

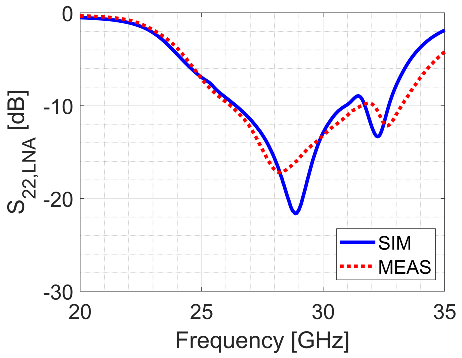
3.3 Measured performance parameters

In this section, the performance (measurements) of the LNA is discussed. Three performance metrics are included, namely small signal behavior (expressed in S-parameters), linearity and noise. These are measured within a 50 Ω environment. Note that the source impedance of the PD does not equal 50 ohm so leading to a distorted interpretation. Therefore, S-parameters need to be transformed.

Additionally, it is also important to notice that during measurement the DC pads of the LNA are connected to PCB traces by using chip capacitors of 10 and 100 nF for additional decoupling and all DC lines for biasing the amplifiers are connected to the same power supply. To combine the photoreceiver with the antenna array, the same decoupling capacitors need to be integrated as well and the amplifier's power supply can be supported by one feed line.



(a) $|S_{21}|$ parameter (b) $|S_{11}|$ parameter



(c) $|S_{22}|$ parameter

Figure 3.4: low noise amplifier: measured and simulated S-parameters [43]

Fig. 3.4 shows the measured S-parameters for a 2 V drain supply. The measured gain, represented by $|S_{21}|$, lies between 24.0 to 23.7 dB in the 27.5 GHz to 29.5 GHz range, which corresponds to a 884 and 788 V/A transimpedance gain (Z_t) from the current source I_{PD} to a 50 Ω load. Taking into account the responsivity of the adopted photodetector (0.8 A/W at 1550 nm), a conversion gain of 707 to 630 V/W is obtained from the input of the photodetector to a 50Ω load. The external conversion gain from the fiber to the output of the LNA is 224 to 199 V/W due to the 5 dB coupling loss caused by the grating coupler. This can be enhanced by making use of edge coupling to reduce the coupling loss to about 1.2 dB, which would result in a conversion gain of 536 to 478V/W.

The input and output reflection coefficients, respectively $|S_{11}|$ and $|S_{22}|$, are below -14.3 and -14.4 dB respectively in the [27.5–29.5] GHz range. The -10 dB bandwidth covers [24.3-30.5] GHz at the input and [26.2-31.6] GHz at the output.

From the $|S_{22}|$, the output impedance of the photoreceiver can be extruded. This is an important characteristic for further use in this research. As the photoreiver will be connected to an antenna array element, this will tell if a matching network between these two components is needed or not. Matching can be done in two ways. One way is by adjusting the design of the antenna element to have an input impedance that matches the photoreceiver output impedance. But this results in a very specific design, hence the antenna will not be easily scalable and transferable to other frequencies or photoreceivers. The other way is by designing a matching network that will be placed between the photoreceiver and antenna element. This is further explained in Chapter 4.

Table 3.1 gives an overview of the measured performance metrics of the LNA.

Linearity is expressed in terms of output referred third order intercept point (OIP3) and output referred 1-dB compression point (O1dBCP). Measuring is done by applying 2V or 3V drain supply, resulting in respectively 160 mW and 303 mW power consumption. The two tone measurement is done at 28.5 GHz with a 20 MHz tone. The measured OIP3 levels are 22.2 dBm at 2V supply and 26.5 dBm at 3V supply. The measured O1dBCP levels are 10.2 dBm at 2V supply and 13.9 dBm at 3V supply. Onward, the 2 V and 3 V supply can be addressed as *low power consumption* or *high linearity* setting respectively.

Noise is expressed as the input-referred current noise, which is a more straightforward interpretation of the sensitivity of the photoreceiver. For the discussed LNA within the targeted frequency band, 2V and 3V drain supply result in respectively an input-referred rms current noise below 11.1 and 11.3 $\text{pA}/\sqrt{\text{Hz}}$.

Passband, 3dB	Input ref. current noise	Gain	Linearity	DC power
23.5 GHz-31.5 GHz	11.1 pA/$\sqrt{\mathrm{Hz}}$	S_{21} = 24 dB, Z_T = 884 Ω	OIP3 = 22.2 dBm	160 mW [2V]
	11.3 pA/$\sqrt{\mathrm{Hz}}$		OIP3 = 26.5 dBm	303 mW [3V]

Table 3.1: Summary of low noise amplifier measurements

Chapter 4

On-chip Antenna Array

As discussed in Chapter 1, the antenna array is designed as an AoC. First, in section 4.1 the design and simulation of a single element is elaborated. What follows is the forming an array with this element. The design and simulation of this array is discussed in section 4.2. In section 4.3 the practical fabrication of the antenna and used techniques are clarified.

4.1 Single element

Designing an antenna array starts by first designing the single antenna element. From the *pattern multiplication* for arrays of identical elements [52], given by:

$$\mathbf{E}(total) = [\mathbf{E}(\text{single element})]X[\text{array factor}] \tag{4.1}$$

Expressing that the far-field radiation pattern of the total array is defined by the radiation pattern of the single element and the array factor. The array factor is already discussed in section 2.3, where the factor equals '1' depending on the desired steer angle (θ_0).

To get the maximum achievable steer angle of the array as great as possible, the beamwidth of the single element has to be as wide as possible. Beamwidth will be expressed using the half power beam width (HPBW) further on. Another important metric will be the front-to-back ratio, as electromagnetic interference with the components on the back of the antenna should be avoided. A front-to-back ratio of at least -10 dB is desired.

Other requirements on the single elements are bandwidth and efficiency. Bandwidth should be at least 2 GHz with a center frequency of 28.5 GHz. This translates more specifically in matching the antenna to 50 Ω in the frequency range of [27.5 - 29.5] GHz. Matching is defined as a reflection coefficient magnitude $|S_{11}|$ below -10 dB, which results in less than 10% mismatch loss. Total efficiency η_{tot} should be at least 90%, this includes radiation efficiency and mismatch loss. To avoid grating lobes when the antenna is used in an array, the antenna dimensions should be equal or smaller then $\lambda_0/2$, which will be explained in section 4.2.

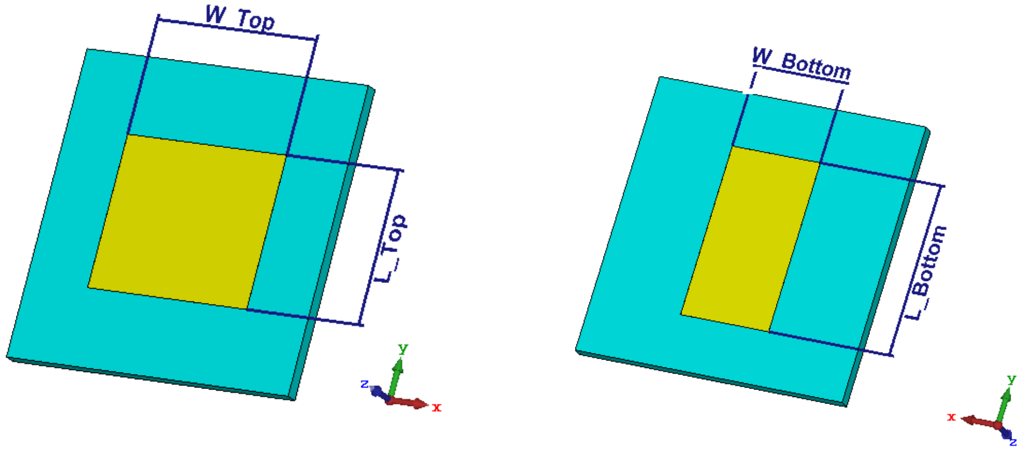
4.1.1 Antenna topology

The single element antenna is based on a hybrid integration strategy for compact, broadband and highly efficient mmWave on-chip antennas designed by Quinten Van den Brande [53]. In this design a cavity-backed stacked patch antenna is implemented on a 600 μm-thick silicon substrate by using air-filled substrate-integrated-waveguide (AFSIW) technology. A hybrid approach is adopted in which the antenna feed and an air-filled cavity are integrated on chip and the stacked patch configuration is implemented on a high frequency PCB laminate that supports the chip, namely Rogers *RO4350B*® ($\epsilon_r = 3.66.$, $\tan\delta = 0.0031$) [54]. A schematic representation of the single element antenna is shown in Fig. 4.1.

The antenna topology consists out of three ”parts”: two stacked patches, a metallic air-filled cavity and a microstrip feed on the bottom of the antenna. The three parts are more explained below.

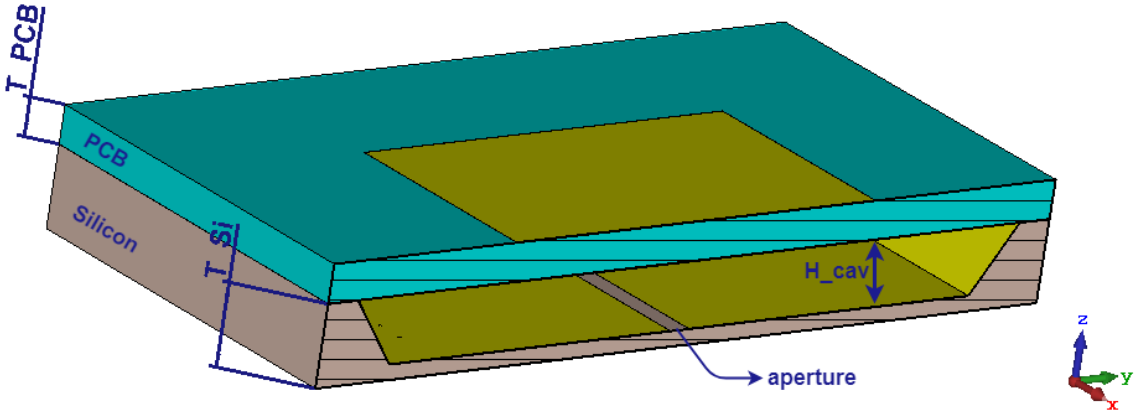
Stacked patches

These patches are responsible for radiating the electromagnetic fields. Each patch forms a microstrip patch antenna. These antennas can be modeled as a resonating cavity between a ground plane and the patch itself, where the radiation leaks from the edges.

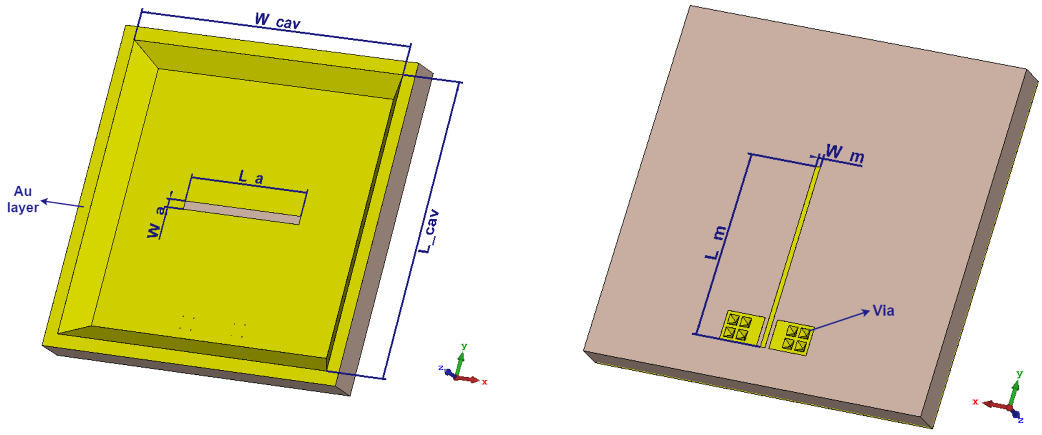


(a) PCB top view

(b) PCB bottom view



(c) Cross-section of the single element antenna



(d) Wafer top view

(e) Wafer bottom view

Figure 4.1: Schematic representation of the single element antenna

Therefore the resonating frequency of these patches depends on its dimensions given by [52]:

$$f_{res,mnp} = \frac{c}{2\pi\sqrt{\epsilon_r}}\sqrt{(\frac{m\pi}{h})^2 + (\frac{n\pi}{L})^2 + (\frac{p\pi}{W})^2} \tag{4.2}$$

with c speed of light, ϵ_r the relative permeability of the substrate, h the distance between patch and ground plane, L the patch's length and W the patch's width. By choosing the appropriate patch dimensions the resonant frequency can be tuned. By using two patches the bandwidth of the antenna can be significantly enhanced. The two patches can be designed for two different resonance frequencies. If these two resonance frequencies are tuned in the proximity of the center frequency of 28.5 GHz the bandwidth is increased [55, 56, 57].

Metallic air-filled cavity

Due to the poor high frequency properties of silicon, mentioned in Chapter 1, a cavity is inserted beneath the patches. As a result, the electromagnetic fields of the stacked patches reside in an air substrate for the most part, hence a low-loss antenna performance is achieved over a large bandwidth and surface wave excitation is strongly suppressed. The skew edges, creating angles of 54.74°, are due to the wet etching using potassium hydroxide (KOH), which is selective to the (100) crystal lattice of silicon and will be further explained in 4.3. After etching the cavity a gold (Au) layer is sputtered on the substrate to form a uniform ground plane. By doing so, the back of the antenna is shielded from the radiating fields, yielding a good front-to-back ratio. The sidewalls of the cavity have a Au layer as well, resulting in full metallic sidewalls. The full metallic sidewalls make the design almost independent of the substrate's dielectric properties. Downside of AFSIW is the increase in effective wavelength, making the design larger [58, 59].

Microstrip feed

The microstrip is responsible for feeding the antenna and is supported by the silicon substrate. On one end it is wire bonded to the photoreceiver output. To avoid unwanted inductance induced by bond wires, the microstrip line should be placed as close as possible to the LNA, making the bond wires as short as possible. On the other end, the microstrip couples the electromagnetic fields to the stacked patches through a rectangular aperture in the ground plane of the metallic air-filled cavity. The rectangular aperture and the tuning stub, being the end piece of the microstrip, allows for an optimization of the front-to-back ratio while still maintaining sufficient bandwidth [53].

Next to the end of the microstrip line two ground pads are placed to form a ground-signal-ground (GSG) pad, which was provided to perform RF measurements. The ground pads contain vias that penetrate the silicon wafer to the cavity on the other side of the wafer. These are needed to make an electrical connection to the ground plane of the cavity beneath it. These ground pads are not necessarily needed anymore in the antenna array, but vias will still be needed to make an electrical connection.

Important to note is that the substrate thickness of the single element antenna designed here is not 600 µm but 540 µm because this is the wafer thickness that is available in the clean room facility. Substrate thickness beneath the cavity is kept 100 µm, and therefore the cavity height is adjusted to 440 µm.

4.1.2 Simulation

All simulations of the single element are done using the frequency domain solver of CST Microwave Studio. In Fig. 4.2 the simulated $|S_{11}|$ parameter is shown. In the desired operating frequency band the antenna is well matched to a 50 Ω load. The input reflection coefficient even stays below -15 dB. The obtained -10 dB bandwidth is ranging from 27.226 to 30.837 GHz, or 3.61 GHz.

In Fig. 4.3 the radiation pattern of the single element antenna is shown. The left plot is for $\phi = 0$, which is the view perpendicular to the microstrip line feed or the H-plane, and the right plot is for $\phi = 90$, or the E-plane. The realized gain is 6.83 dBi in both planes. The half-power beamwidth in the H-plane is 87.1°, and in the E-plane 79.9°. The front-to-back ratio is for both planes -15.7 dB.

The total efficiency obtained by the antenna is 92.6% at 28.5 GHz

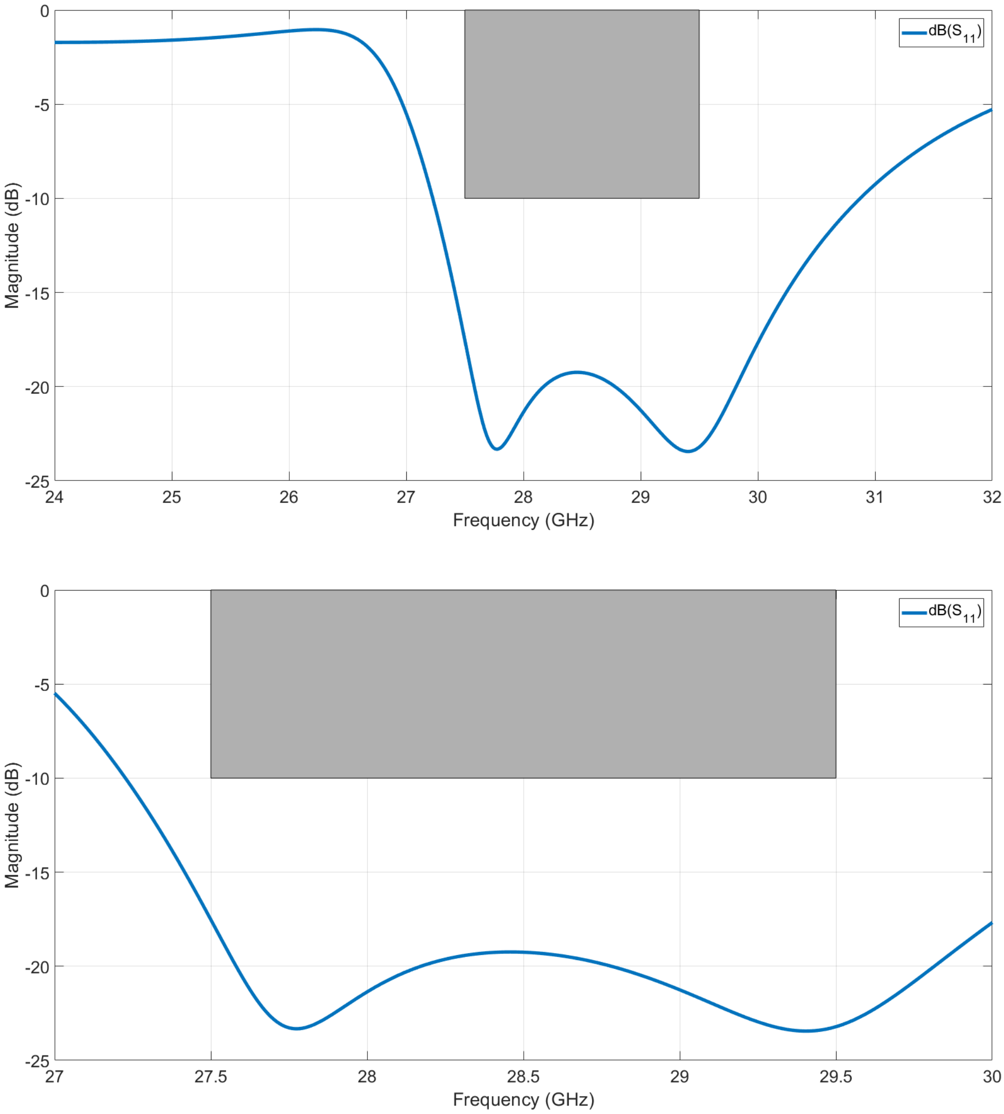


Figure 4.2: Simulated $|S_{11}|$ parameter of the single element antenna

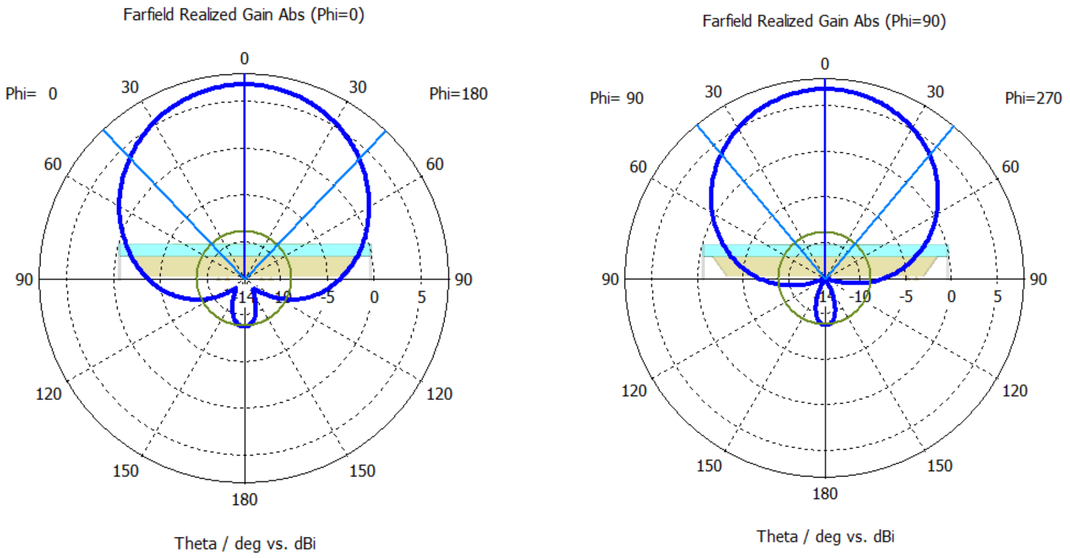


Figure 4.3: Simulated radiation pattern of the single element antenna, at 28.5 GHz

From the simulations it can be concluded that the designed single antenna has good performance metrics to be used in an antenna array.

4.2 Array configuration

In this section the designed single element antenna from section 4.1 will be used to form an 4-element ULA. First the design specifications and decisions will be discussed in subsection 4.2.1. In subsection 4.2.2 the antenna array simulation results are elaborated.

4.2.1 Design decisions

When designing the antenna array, several design decisions needed to be made. These are listed below:

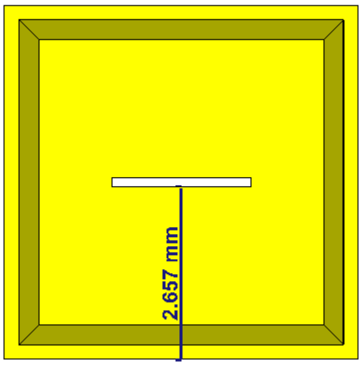


Figure 4.4: Available place for LNA on single element antenna

Photoreceiver placement:

As first, the placement of the photoreceiver needed to be taken into account. The single element antenna has as footprint 5.00 mm x 5.00mm, which is defined by the cavity width and length. To avoid grating lobes, the antenna footprint should be smaller than $0.5\lambda_{min}$ x $0.5\lambda_{min}$ or 5.450mm x 5.450mm with λ_{min} the free-space wavelength at 29.5 GHz [52, 53]. So we can extend the substrate around the cavity with 225 µm to have more free area where the photoreceiver can be placed.

In Fig. 3.2 the dimensions and configuration of the photoreceiver are shown. Here is seen that the needed space in the y-direction is 5.274mm. With an antenna length of 5.450mm, the free space between aperture and end of the antenna is 2.657mm. This is illustrated in Fig. 4.4. Bearing in mind space for the ground pads with width 450 µm and a 100 µm minimal spacing between ground pad and aperture (to take in account processing errors that can occur), gives a resulting free space of 2.107mm.

Unfortunately this is not sufficient to place the photoreceiver on the single element antenna. As a solution the substrate is extended on the side of the antenna where the photoreceiver can be placed on with 3.167mm. The resulting single element antenna is shown in Fig. 4.5.

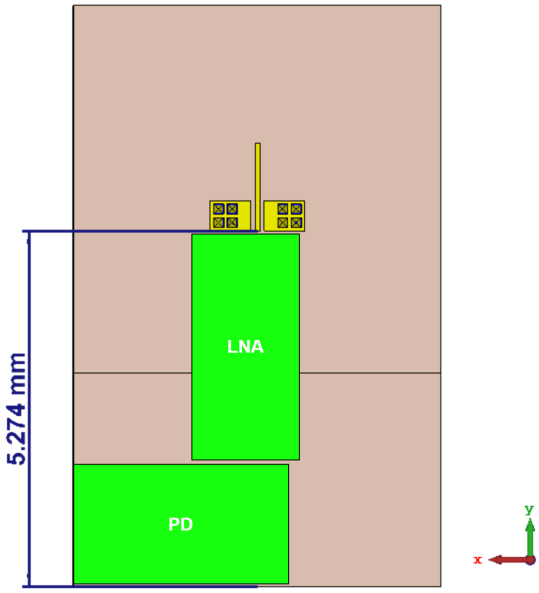


Figure 4.5: Single element antenna with space provided for placing the photoreiver

As a result the microstrip line (L_m) length is decreased as well to create space. This influences the antenna impedance and as a result the antenna is not matched to $50\,\Omega$ anymore in the same frequency range, because the microstrip line acts as a transmission line. So changing its physical length changes its electrical length, and this changes the phase of the transmission line impedance. Therefore, the antenna single element impedance seen through this transmission line changes as well, as can be seen in Fig. 4.6. Decreasing the length of the microstrip line causes the Smith chart plot of the antenna single element impedance to rotate anti-clockwise. Fig. 4.7 plots the resulting $|S_{11}|$ parameter of the single element antenna. The resulting reflection coefficient bandwidth is shifted towards lower frequencies.

To shift the reflection coefficient bandwidth back to the wanted frequency range of [27.5 - 29.5] GHz, an optimizer is used to tune the aperture length and width, L_a and W_a. The optimizer algorithm used is Nelder Mead Simplex algorithm, as this is a relative simple and robust algorithm for finding optimal solutions [60]. The goal of the optimizer is set to -20 dB $|S_{11}|$ in the frequency range of [27.5 - 29.5] GHz to get back as close as possible to the original bandwidth.

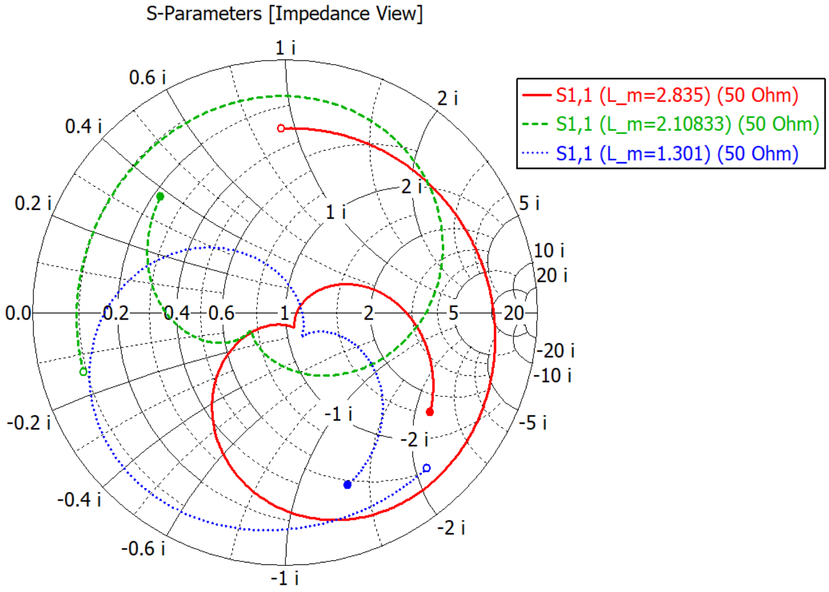


Figure 4.6: Smith chart of antenna impedance with varying microstrip line lengths

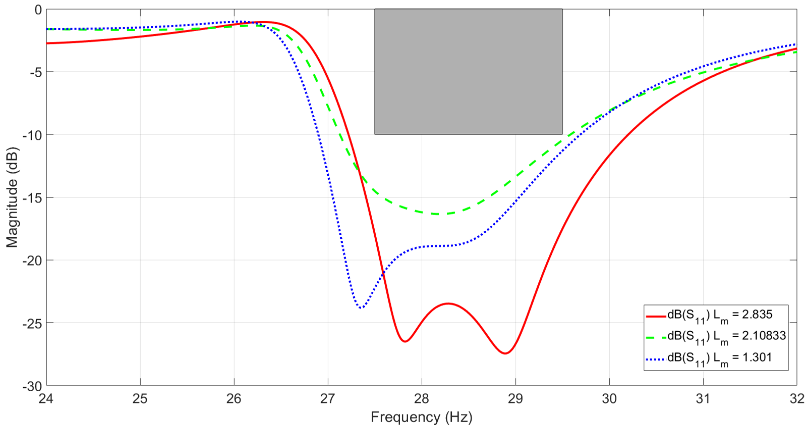


Figure 4.7: $|S_{11}|$ plot of single element antenna with varying microstrip length

The solution presented is to change the aperture area from 2.15mm by 0.14mm to 2.635mm by 0.154mm. Hence, making the aperture slightly longer and wider results in a decrease in front-to-back ratio of 2 dB. The resulting reflection coefficient is shown in Fig. 4.8.

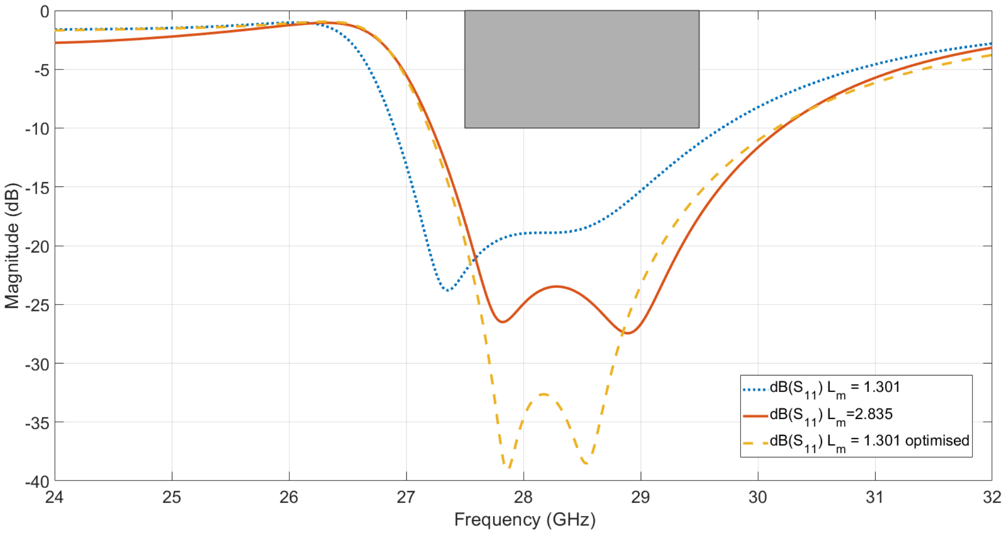


Figure 4.8: $|S_{11}|$ plot of single element antenna with optimized aperture dimensions

This reflection coefficient is then used to plot the mismatch loss between the photoreceiver output impedance and antenna input impedance, using Keysight ADS. The photoreceiver output impedance follows from section 3.3. The resulting mismatch loss is plotted in Fig. 4.9. Here, it can been seen that the mismatch loss is below -1 dB in the frequency range of interest. Therefore, it is concluded no matching network between photoreceiver and antenna is needed. Note that the reflection coefficient shown is the reflection between photoreceiver and antenna.

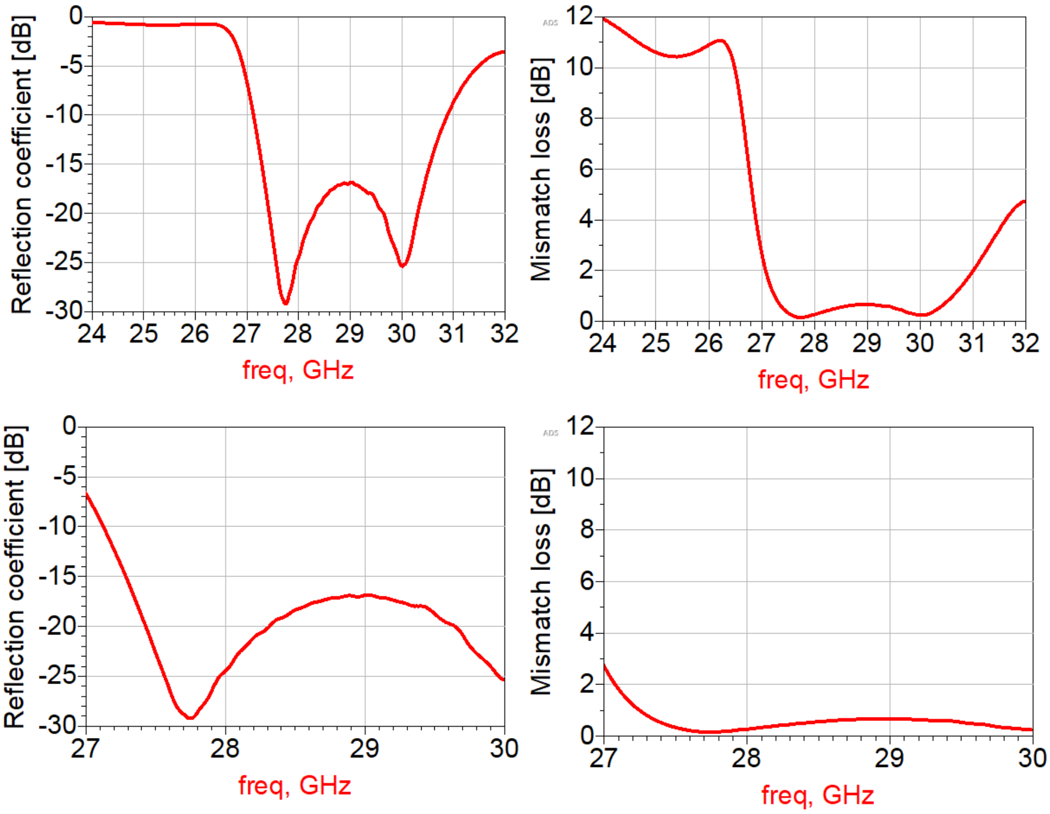
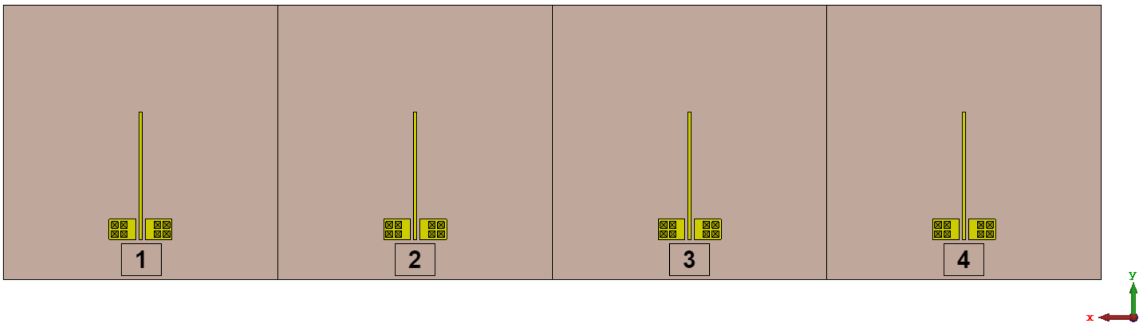


Figure 4.9: Mismatch loss between photoreceiver and antenna

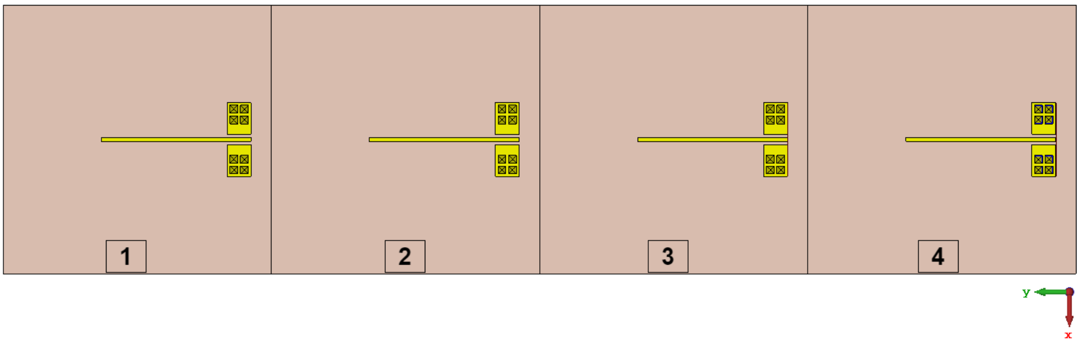
Orientation of the elements:

Second design decision that occurred was how to orient the elements. Orientation can be done in a 1x4 (Fig. 4.10a) or 4x1 (Fig. 4.10b) configuration, with antenna ports indicated as (1,2,3,4) going from the most left antenna element to the most right.

In Fig. 4.11 the passive S-parameters of both orientations are compared, with S_{ii} the reflection coefficient of the i$^{\text{th}}$ antenna element when only the i$^{\text{th}}$ antenna element is excited and the other elements are perfectly matched. When all antenna elements are excited simultaneously the S-parameters are called active S-parameters or F-parameters. This occurs when beam steering is applied to the antenna array. Only $|S_{11}|$ and $|S_{22}|$ are shown in Fig. 4.11a because of the symmetry of the arrays they are equal to $|S_{44}|$ and $|S_{33}|$ respectively. While S_{ij} denotes the isolation between antenna element i and j. This metric is explained further on.



(a) 1x4 array configuration

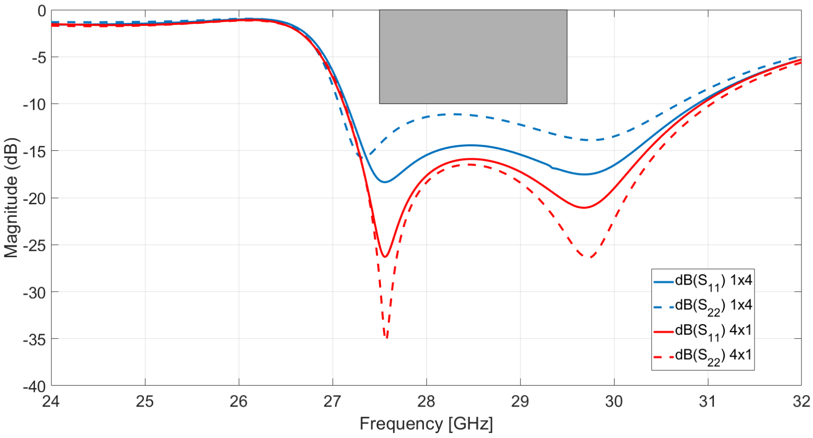


(b) 4x1 array configuration

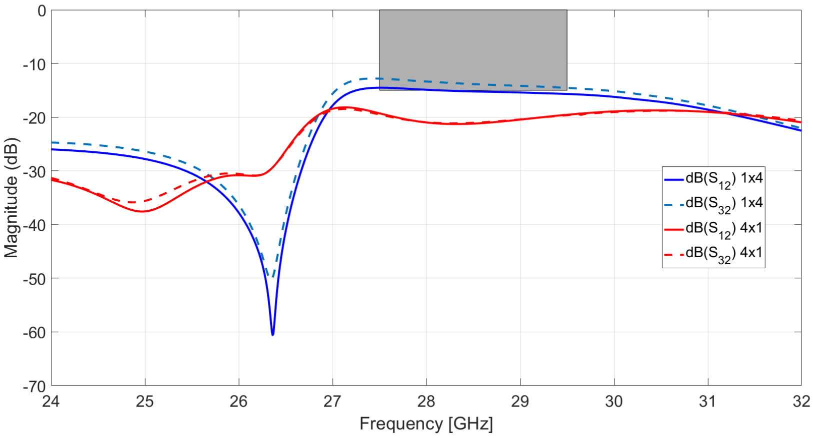
Figure 4.10: Different array configurations

In Fig. 4.11b, isolation between the antenna element on the left and on the right right of the second element in the array is shown, respectively S12 and S32. Both array configurations are simulated using a inter-element distance of $\lambda_{min}/2$, with λ_{min} the free-space wavelength at a frequency of 29.5 GHz .

From Fig. 4.11 it can be concluded that the 4x1 configuration exhibit better reflection coefficients and better isolation between adjacent antenna elements. Note that the 1x4 configuration isolation curves are not beneath the desired limits, but this will be solved by changing the inter-element distance.



(a) $|S_{11}|$ and $|S_{22}|$ plot of the 1x4 and 4x1 array configuration



(b) S12 and S32 plot of the 1x4 and 4x1 array configuration

Figure 4.11: Passive S-parameters of the 1x4 and 4x1 array configuration

In Fig. 4.12 the active S-parameters, or F-parameters, are compared for both orientations. For the same symmetry reason only F1 and F2, being the active $|S_{11}|$ and $|S_{22}|$ parameter, respectively, are shown. These plots are simulated for steering broadside, or beam steering with a steering angle θ_0 set to 0°. Both orientations and all F-parameters stay below the -10 dB limit here.

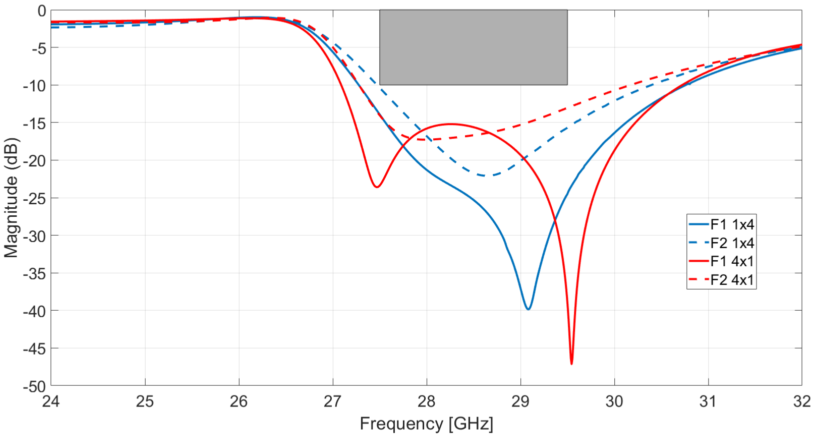


Figure 4.12: F1 and F2 plot of the 1x4 and 4x1 array configuration

Fig. 4.13 and 4.14 are plots that summarizes the far-fields radiation patterns for the different orientations. In Fig. 4.13 the resulting main lobe direction is plotted with respect to the applied steer angle, as well as the optimal curve. For both orientations the main lobe direction starts to deviate from the optimal curve around 30°. This is due that the single antenna element radiation pattern is not omnidirectional but has a half-power beamwidth of 79.9° (radiating at most 3dB power in a range of -39.95° to 39.95°) and as the radiation pattern of the antenna array is defined by pattern multiplication (eq. 4.1) this limits the maximal scanning range. This is not necessarily a big problem. If the beamwidth of the radiation pattern is still wider than the deviation, enough energy is radiated in the desired direction.

Fig. 4.14 shows the realized gain and relative side lobe level for different applied steer angles. The resulting gains for the 1x4 and 4x1 configuration are 12 dBi and 11.8 dBi at a steer angle of 0°, respectively. For the 1x4 configuration this stays the same up to an angle of 45° and then drops 2.49 dB. The 4x1 configuration deviates around 30° and drops 3.6 dB. This increase in gain, compared to the single element antenna (5.17 dB in the case of 1x4 orientation and 4.97 dB in the 4x1 orientation) is the result of *pattern multiplication*, expressed by equation 4.1. Note that the realized gain is plotted here, which includes mismatch losses as well. Therefore, not a 6 dB gain is achieved here that is predicted by equation 4.1. This also explains the difference between both configurations as the 4x1 configuration is slightly worse matched as seen by the F-parameters Fig. 4.12.

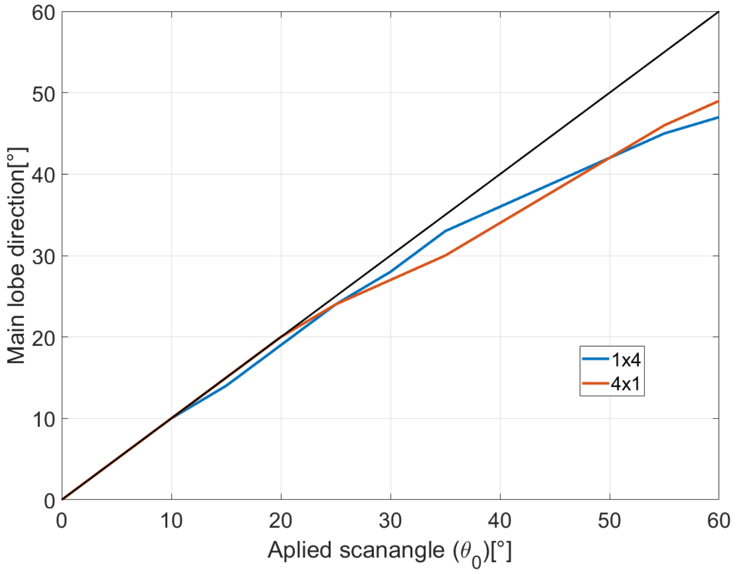


Figure 4.13: Applied steering angle θ_0 and the resulting main lobe direction for the 1x4 and 4x1 array configuration

The relative side lobe level is the difference in dB between the main lobe and the second greatest lobe in the radiation pattern. In Fig. 4.14 can been seen that when steering away from broadside, the relative side lobe level decreases. This is due to grating lobes, which will be explained further on. This effect can be bad for the operation of the antenna array, as the relative side lobe level gets close to 0, meaning that the side lobe level is as high as the main lobe, resulting in energy being radiated by the side lobe in an unwanted direction. The relative side lobe level for both configurations are more or less the same, so based on this no orientation is preferred.

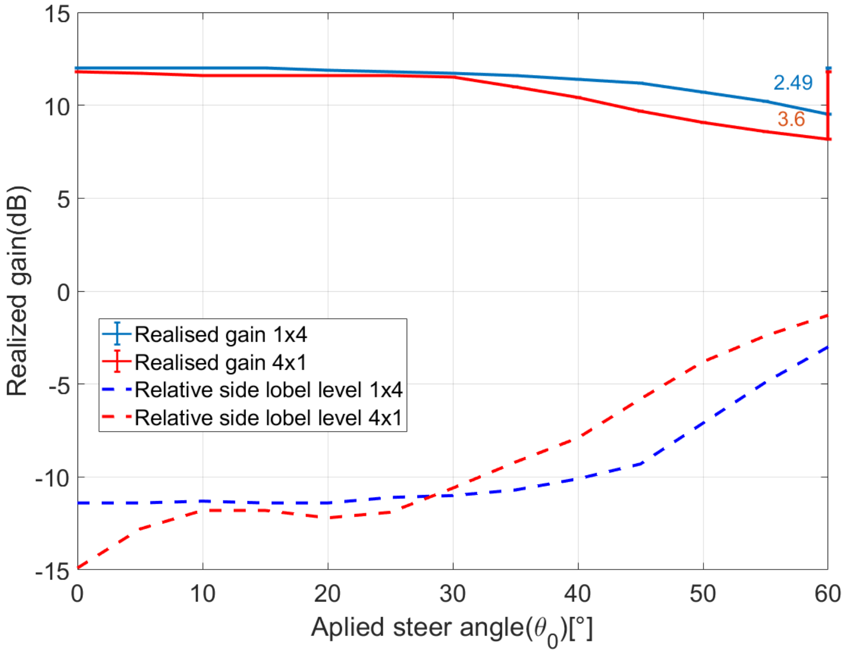


Figure 4.14: Realized gain and relative side lobe level for different applied steering angle θ_0 for the 1x4 and 4x1 array configuration

As a result of the extension of the substrate of the single element antenna in the -y direction for placement of the photoreceiver, as seen in Fig. 4.5, using the 4x1 array configuration will results in a larger inter-element distance. The minimum inter-element distance that could be used is $0.85 * \lambda_{min}$. Due to avoiding grating lobes, the maximum achievable steer angle would be ±10.2°. This will be explained further on. Also the feeding of the photoreceiver, as well as the coupling of the optical fibers is easier in the 1x4 configuration than the 4x1, therefore the 1x4 configuration is chosen.

For the same reason of the substrate extension, going from a linear to a planar array configuration will not be that straightforward. Hence, this is listed as future work.

Inter-element spacing:

The third design decision is the inter-element distance. This decision results in a trade-off between the maximum grating lobe-free steer angle, mutual coupling and structural stability of the antenna.

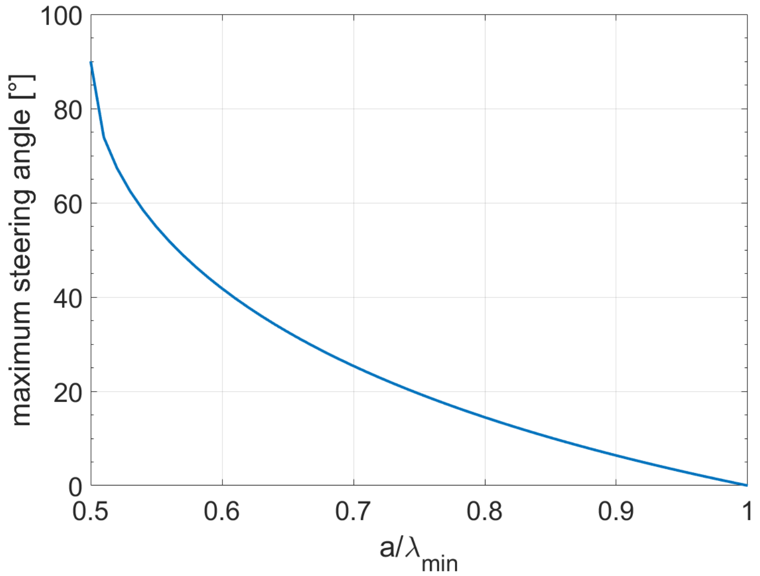


Figure 4.15: Maximum steer angle w.r.t. inter-element distance depending on grating lobes

To avoid grating lobes, the steer angle should be limited by the following formula:

$$\frac{a}{\lambda_{min}} = \frac{1}{1 + sin|\theta_{0,max}|} \tag{4.3}$$

With a the inter-element distance, λ_{min} the free-space wavelength and $\theta_{0,max}$ the maximal achievable steer angle, as depicted in Fig. 4.16. Fig. 4.15 is a plot of the max. achievable steer angle with respect to the inter-element distance. Increasing the inter-element distance decreases the max. achievable steer angle, so the distance must be as small as possible to achieve the greatest scanning range.

Placing elements closer together results in more mutual coupling between elements. Hence, energy injected in one element will partly flow towards other elements and will not be radiated, resulting in losses. To reduce these losses, the inter-element distance should be increased.

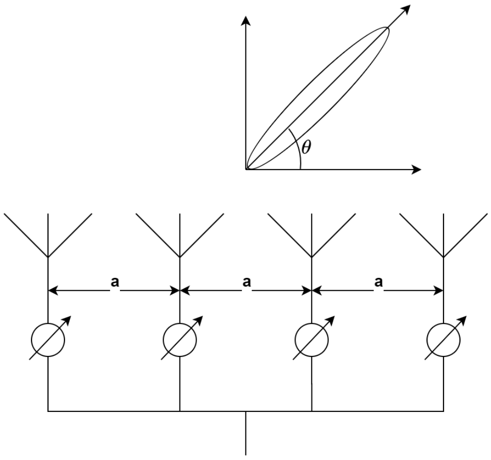
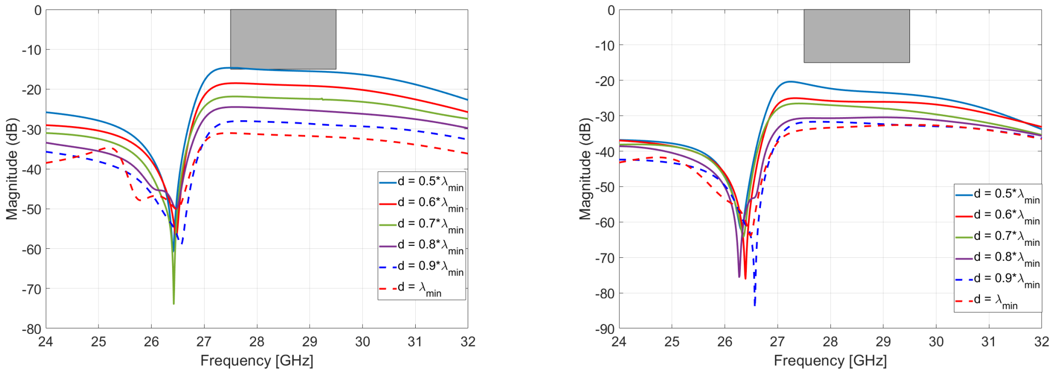


Figure 4.16: Schematic representation of grating lobe-free beam steering

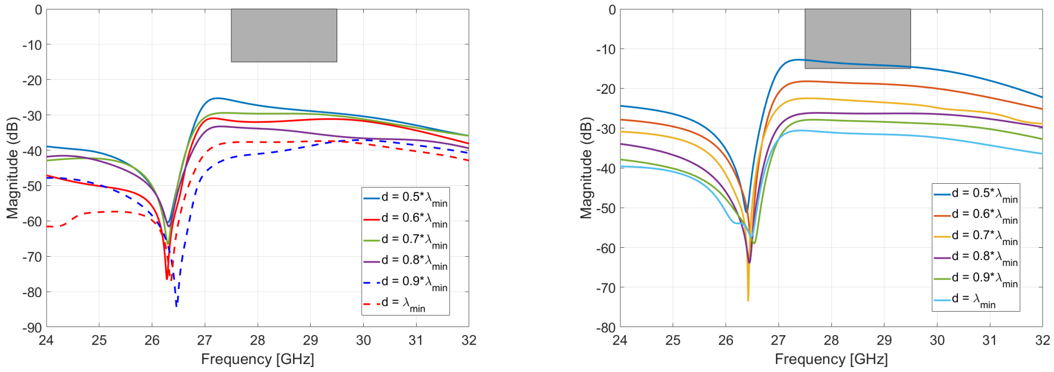
a = inter-element distance, θ = steer angle

A metric to measure these power losses are the S_{ij} (i $\neq$j) parameters, denoting the power inserted in port j relative to power coming out of port i, or isolation between port i and j. Good isolation between elements are considered here as S_{ij} smaller than -15 dB. Fig. 4.17 shows some of these isolation values between port 1 and 2 (S21), 1 and 3 (S31), 1 and 4 (S41), 2 and 3 (S32). Only an inter-element distance of 0.5*λ_{min} isolation between adjacent ports gets above the -15 dB limit. Isolation between the ports of the antenna elements that have one or more antenna elements between them is always ensured regardless of the inter-element distance.
Mutual coupling also influences the impedance of a single antenna element, as this cannot be interpreted anymore as the impedance of a stand-alone antenna element but a combination of its impedance and those of adjacent antenna elements [52], resulting in different input reflection coefficients and possible mismatch between antenna element and 50 Ω load. In Fig. 4.17 the isolation between the first element and all the other elements is plotted for increasing inter-element distance. Concluded from these results the inter-element distance should be at least 0.6*λ_{min}.

Increasing the inter-element distance also results in a larger antenna, which is more robust and structural stable, making processing and handling the antenna easier. Also, more substrate is available between adjacent antenna elements. Hence, more space is provided to place BGA balls. The use of these balls will be explained in section 4.3.



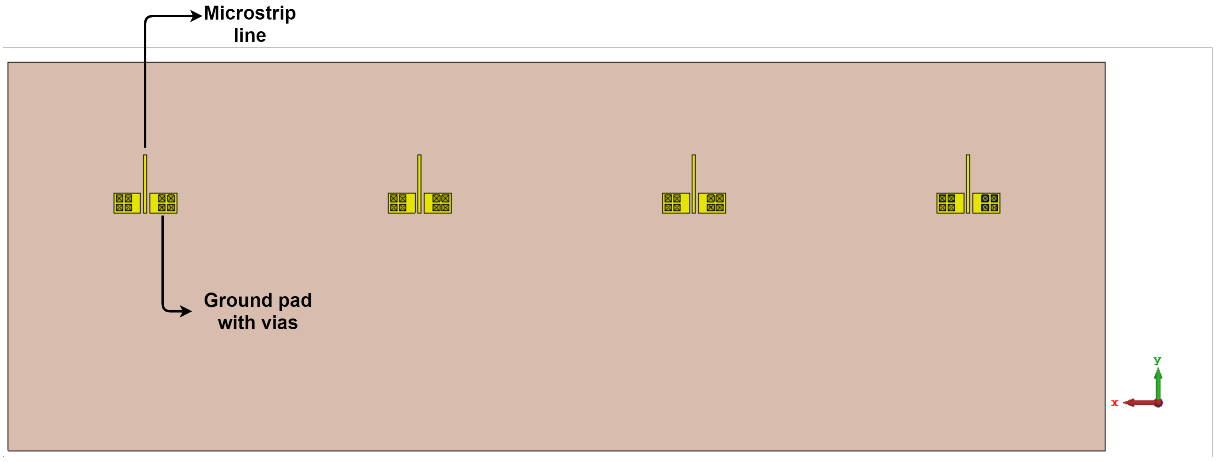
(a) S21 parameter (b) S31 parameter



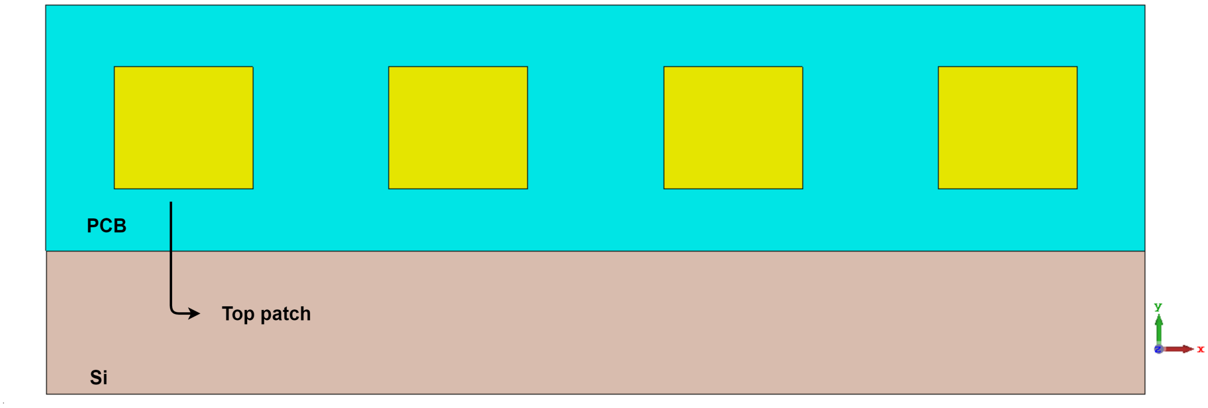
(c) S41 parameter (d) S32 parameter

Figure 4.17: Different isolation values of the antenna array with varying inter-element distance

Based on these three criteria $0.6^{*}\lambda_{min}$, or 6.0974mm is chosen as inter-element distance (a). This results in good isolation between elements, a stiffer antenna array and a grating lobe-free scanning range of ±41.81°. The resulting antenna array is shown in Fig. 4.18, by a top and bottom view. Resulting antenna dimensions are summarized in Table 4.1.



(a) Top view



(b) Bottom view

Figure 4.18: Top and bottom view of the antenna array

parameter		Value[mm]
Top patch length	L_{top}	2.710
Top patch width	W_{top}	3.080
Bottom patch length	L_{bottom}	3.350
Bottom patch Width	W_{bottom}	1.800
PCB thickness	T_{PCB}	0.254
Patch thickness	T_{patch}	0.035
Aperture length	L_a	2.635
Aperture width	W_a	0.154
Microstrip length	L_m	1.301
Microstrip width	W_m	0.074
Ground pad length	L_{viapad}	0.600
Ground pad width	W_{viapad}	0.450
Ground pad spacing	S_{viapad}	0.063
Via length	L_{via}	0.150
Via width	W_{via}	0.150
Via spacing	S_{via}	0.050
Cavity height	H_{cav}	0.440
Cavity length	L_{cav}	5.000
Cavity width	W_{cav}	5.000
Silicon wafer thickness	T_{Si}	0.540
Gold thickness	T_{Au}	0.001
Inter-element distance	a	6.097
Array configuration		1x4

Table 4.1: Summary of the antenna array dimensions

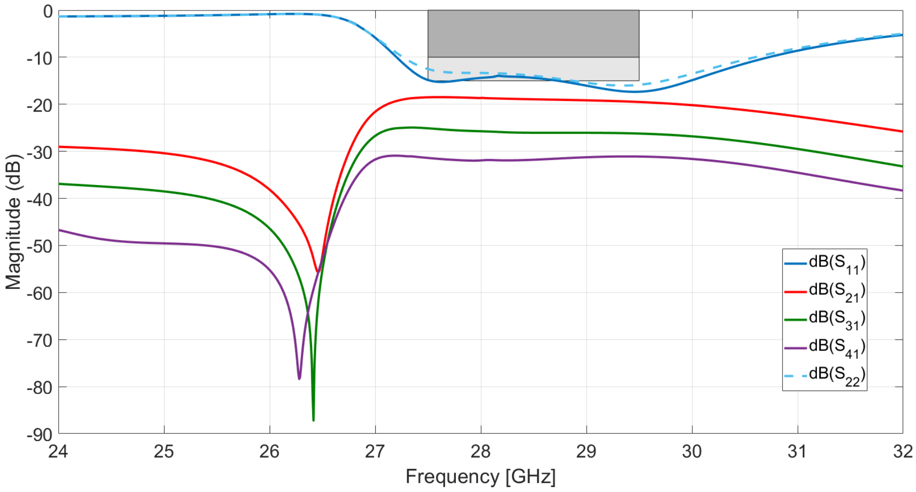


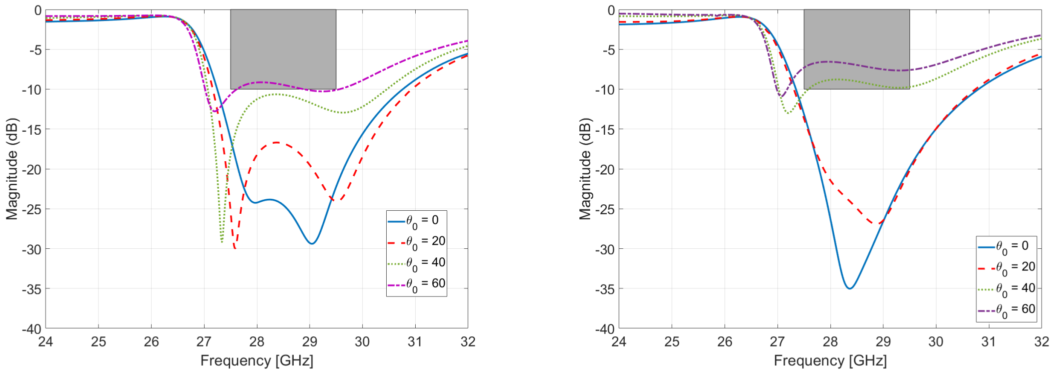
Figure 4.19: S-parameters of the antenna array

4.2.2 Simulation

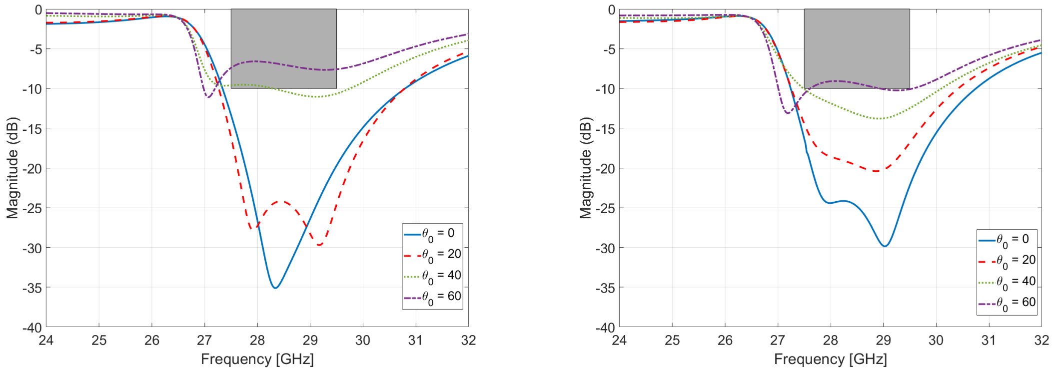
In this subsection the simulation results of the final antenna array are discussed. Simulation is done for different steer angles, ranging from 0° to 60° in steps of 10°. First, the obtained passive and active S- and F-parameters are observed. Second, the resulting far-field radiation patterns.

From the passive S-parameters depicted in Fig.4.19, the bandwidth can be defined as the frequency range where $|S_{11}|$, $|S_{22}|$, $|S_{33}|$ and $|S_{44}|$ are all below -10 dB. Here also only $|S_{11}|$ and $|S_{22}|$ are plotted because of symmetry reasons. The dark gray box indicates the -10 dB limit for the reflection coefficients and the light gray indicates the -15 dB isolation limit. All S-parameters are below the imposed limits. The resulting bandwidth is 27.27 to 30.61 GHz, or 3.34 GHz.

The F-parameters are summarized in Fig. 4.20. These are plotted for a steer angle of 0°, 20°, 40° and 60°. It can be concluded that the antenna gets mismatched when steering at 60°, so steering at this angle would result in lot of return losses (about 25% input return loss at element 2 and 3, and 10% at element 1 and 4). For 40° only F2 and F3 reach the -10 dB limit, also resulting in return loss but not that much as at 60°(about 10% at element 2 and 3). This also results in a decreasing total efficiency of the antenna array when steering away from broadside.



(a) F1 parameter (b) F2 parameter



(c) F3 parameter (d) F4 parameter

Figure 4.20: F-parameters of the antenna array, for steer angle of 0°, 20°, 40° and 60°

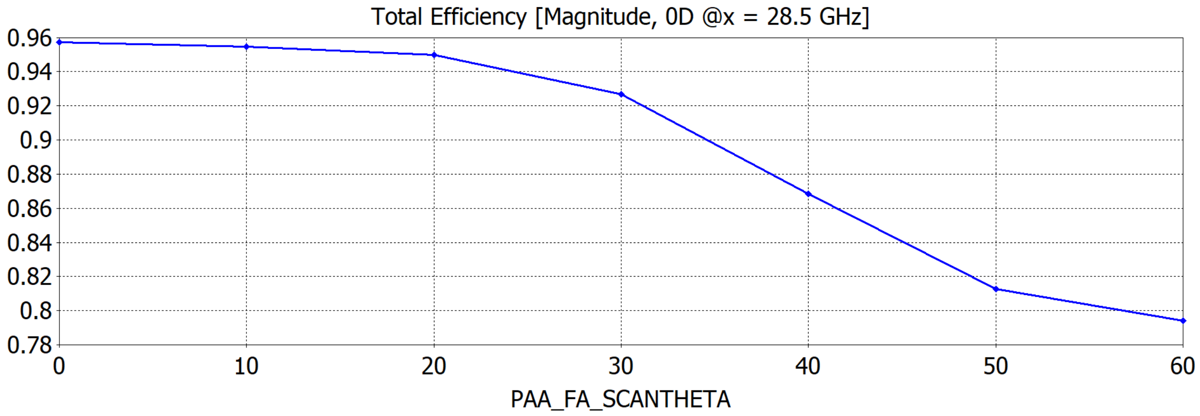
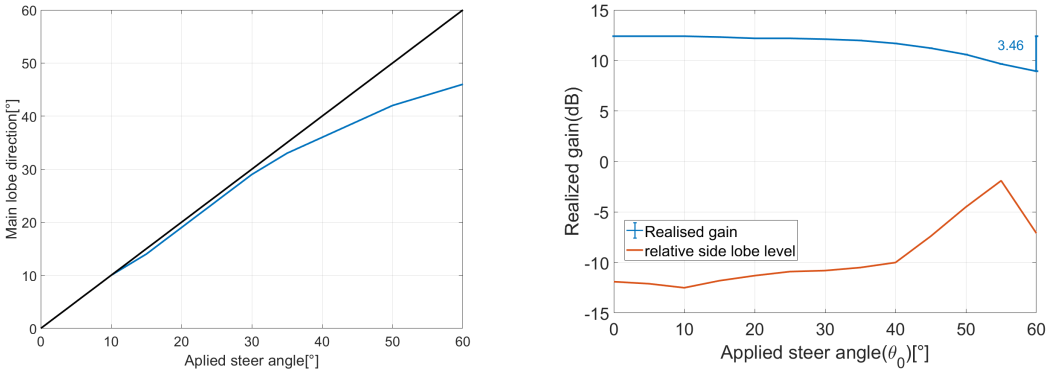


Figure 4.21: Total efficiency of the antenna array for different steer angles

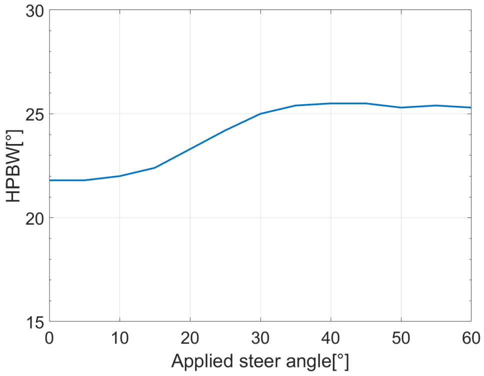
The resulting total efficiency is plotted in Fig. 4.21. Within a scanning range of [-40°, 40°] the total efficiency stays above 86%.

Fig. 4.22 is a summary of the radiation patterns of the antenna array for steering angle going from 0° to 60° in steps of 5°. The main lobe direction starts to deviate from the applied steer angle around 35°, as shown in Fig. 4.22a. Fig. 4.22b plots the realized gain and the relative side lobe level. The realized gain at 0° is 12.4 dBi and drops 3.46 dB at 60°. The limit induced by the grating lobe formula given by equation 4.3, for a spacing of $0.6*\lambda_{min}$ would be ±41.81°. Which is visible in the plot of the relative side lobe level (Fig. 4.22b), as it starts to decrease around 40°, meaning grating lobes start to appear in the radiation pattern. The relative side lobe level stays below -10 dB up to 40°. The beamwidth stays more or less the same for different steer angles, around 24°. Fig. 4.23 shows the far-field radiation pattern in a Cartesian plot for steer angle of 0°, 20°, 40° and 60°.



(a) Applied steering angle θ_0 and the resulting main lobe direction

(b) Realized gain and relative side lobe level for different applied steering angle θ_0



(c) Half power beamwidth for different applied steering angle θ_0

Figure 4.22: Far-field radiation pattern summarized for different steer angles

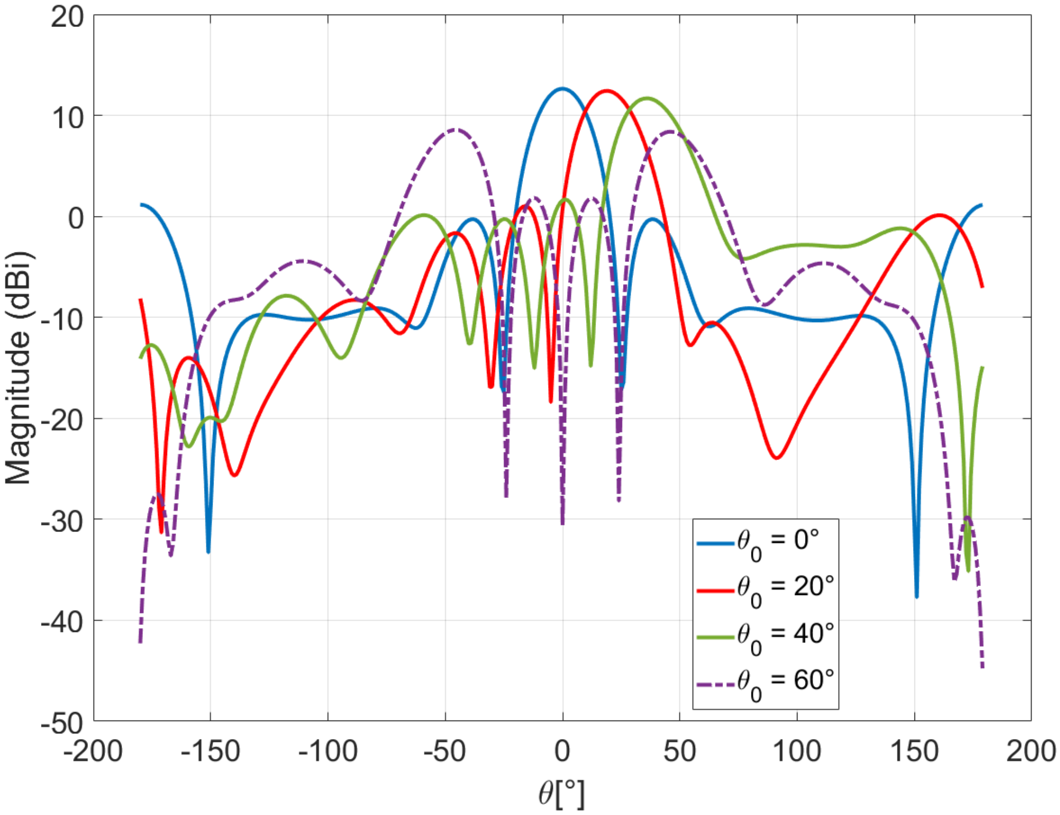


Figure 4.23: Far-field radiation pattern for different steer angles

4.3 Technologies and fabrication

This section explains the technologies and features that are provided to fabricate and employ the antenna array. These features are feeding for the photoreceiver, PCB attachment using BGA and coupling of the optical fibers. In the last section, the procedure for fabricating the silicon chip is described.

As explained above the total system exists out of two parts. A silicon chip, containing the antenna array cavities and microstrip feed lines, and a PCB with the two patches. This PCB will also serve as rigid carrier for the total antenna array. The PCB is extended to an area of 7cm by 9.37cm, so the whole system can be attached to an optical table for measurements. The fabrication of the PCB is done by an external PCB-manufacturer, namely Eurocircuits. The silicon chip is made using different CMOS microfabrication technologies inside the clean-room facilities of Ghent University.

4.3.1 Photoreceiver feeding

To drive the photoreceiver, supply voltages need to be provided. These voltages are needed to feed the transistors in the LNA and to reverse bias the PD. As discussed in Chapter 3 the three transistors inside the LNA can be fed using the same voltage, meaning only one feed line is required to supply this voltage. So for every photoreceiver two feed lines are necessary. Fig. 4.24 shows a close-up of the feed lines present at the top of the chip. Note that 2 mm space is foreseen to place decoupling capacitors, one of 10 nF and one of 100 nF. Each amplifier and PD should be decoupled so 8 decoupling capacitors are needed in total. The feed lines have a header of 0.5mm by 0.5mm. From the headers a wire bond can be soldered to the decoupling capacitors and from the capacitors to the soldering pads present on the LNA.

Note that the ground pads aside the microstrip line are not present anymore. These are substituted by a ground plane that is extending over the whole surface of the chip. Because the bottom of the LNA also has a ground plane attached to it, a good electrical connection is provided by

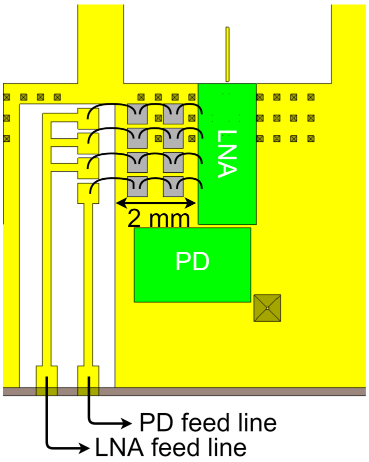


Figure 4.24: Feed lines present on top of the chip

this manner. The 2x2 vias that deliver the connection to the ground plane of the cavity are replaced by a 3x11 array of vias.

The feed lines are also integrated in the PCB and routed towards a pin-header contact, where the needed supply voltages can be applied using a pin-header. The connection between the feed lines on the chip and on the PCB can be done in three ways. The first way is by creating a connection through the silicon wafer by etching vias on the top side through the substrate to the bottom side where a connection with a BGA ball is used as interconnection to the PCB, this is explained in next subsection 4.3.2. The second way is by routing the feed lines on the chip around the edge of the chip and use a BGA ball as connection between chip and PCB. This is possible due to the skew edges of the chip that are created during 'cutting' of the chip out of the silicon wafer. 'Cutting' is done by using the same wet etch technique to form the vias and the cavities. This will be discussed in detail in subsection 4.3.4.
The final way of connecting, more seen as a back-up when the connection around the edge fails, is by wire bonding from the feed line on the chip to the feed line on the PCB. Therefore, the feed line on the chip is made wider when it gets closer to the edge, to have enough space to connect a wire bond. This is also seen in Fig. 4.24.

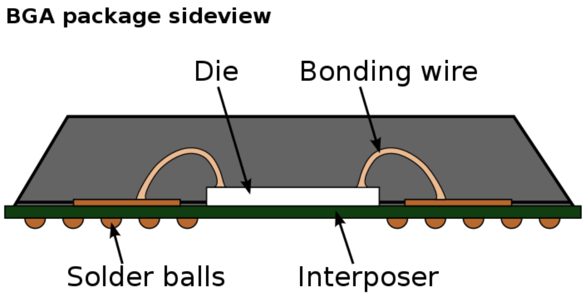


Figure 4.25: Side view of a schematic representation of a BGA package [61]

4.3.2 PCB attachment - BGA

This subsection discusses how the chip is attached to the PCB. In this research the use of BGA as an adhesive will be investigated. BGA is a well known technique for packaging and binding CPU's and IC's to motherboards or PCBs [61]. Fig. 4.25 is a schematic representation of a BGA package. In this research, only the bonding technique of BGA is relevant. This bonding is typically done by attaching first the BGA balls to the package, which are made out of a solder. Second the package is placed on the PCB that has copper pads in a pattern that matches the solder balls and a soldering paste is applied on these copper pads. The assembly is then heated, either in a reflow oven or by an infrared heater, melting the balls and soldering paste. Surface tension causes the molten solder to hold the package in alignment with the circuit board, at the correct separation distance, while the solder cools and solidifies, forming soldered connections between the package and the PCB.

This alignment property is the reason why there is chosen for BGA as adhesive. Because, misalignment of the chip on the PCB has as consequent that the antenna patches are not alignment anymore with the microstrip feed and aperture. Especially a displacement in the y-direction has a significant influence on the bandwidth of the antenna array, as these result in a decreased bandwidth. This is explained in Chapter 5.

Attaching the BGA balls to the chip is done by creating little cavities around the antenna array cavities on the bottom of the chip, indicated in Fig. 4.26. The BGA balls used have a diameter

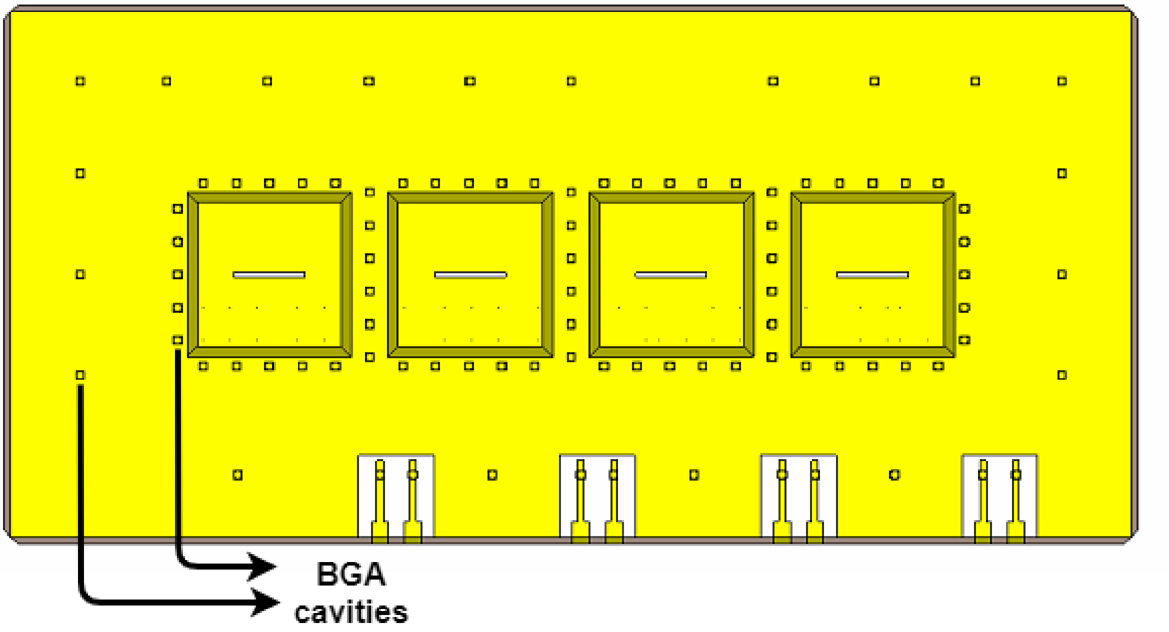


Figure 4.26: Bottom view of the silicon chip

of 250 µm, and the cavities on the chip are designed such that half of the volume of the ball can fit into it. Resulting in cavities of 250 µm by 250 µm.

Attachment to the PCB is done by soldering the balls to the ground plane on the bottom side of the PCB. Here, alignment is ensured by applying a solder mask on the PCB that matches the BGA pattern. A solder mask is also applied to the chip as well by using a benzocyclobutene (BCB) layer that has a cavity pattern in it that matches the BGA pattern. This is explained in detail in subsection 4.3.4.

As an extra advantage, connection through the BGA balls can be used to connect the ground plane of the PCB and the ground plane of the chip. The ground connection is then extended through the silicon wafer by placing cavities of width and length of 638 µm on the top side of the chip, opposite to the cavities placed for BGA attachment. This through connection is shown in Fig. 4.27. This connection is also possible to connect the DC-feed lines on the chip and PCB.

There is a back-up plan if the technique of BGA doesn't provide the needed attachment or fabrication errors occur during BGA placing or reflow. The back-up is using BCB as an adhesive layer. BCB is widely used as adhesive polymer in MEMS technology [62]. Briefly described, BCB is spin-coated on the surface of the silicon chip. The chip is then placed on the PCB

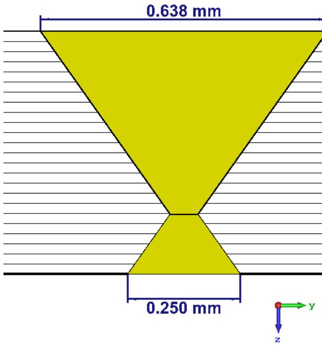


Figure 4.27: Ground connection through silicon wafer

and are pressed together. Afterwards, the assembly is heated to 150° while still being pressed together. After 20 minutes the antenna is finished. The risk here exist that spin-coating BCB on the bottom side of the chip will get stuck inside the antenna cavities and no uniform layer is created.

4.3.3 Fiber coupling

After that the chip is placed on the PCB, the last thing needed for the antenna array to work is of course an input signal. These are applied through four optical fibers that come from the OBFN. Each fiber needs to be coupled to a PD of the photoreceiver. To make the coupling easier a Plexiglas mount will be used to place on the PCB. This mount has two holes in it. One hole fits around the chip and one hole fits around the pin-header. Fig. 4.28 is a schematic representation of this Plexiglas mount. On the mount four supporting blocks and bridge are placed where the optical fibers can be attached to. The supporting blocks have a skew edge so the fibers can land under the optimal angle of 4° on the grating couplers for optimal power transfer to the PD. This mount is attached to the PCB using M1 screws that are placed around the chip. Therefore the feed lines running on the PCB are routed around these screws. The influence on the radiation pattern of the antenna array by these screw heads, that stick out on the bottom side of the PCB, is left as further work.

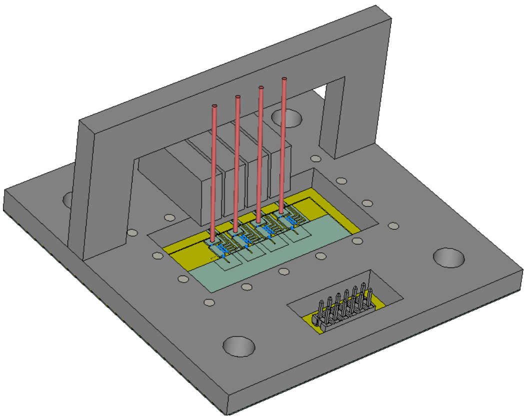


Figure 4.28: Schematic representation of the Plexiglas mount

4.3.4 Clean room procedure

This section is about the Clean room procedure. The following steps explains how all the features are created on the silicon wafer to form the chip. Detailed descriptions of processing steps can be found in previous work of Dennis Maes, appendix A [40]. Appendix A below is an extension to the appendix of Dennis Maes, containing processing steps that are not present in it or that are adjusted. What follows is an outline of the processing steps. These steps are performed on a two-sided polished wafer of undoped silicon that has a layer of 310nm Si3N4 deposited on it, forming a hard mask layer.

1. **Sample preparation**: At first, a sample of size 36cm by 18cm is made using the same techniques as in appendix A.1 [40], by cleaving and rinsing the sample. The cleaving doesn't need to be that precise because in the lithography masks for the top and bottom side a border defined that will 'cut out' the chip out of the sample during wet etching.

2. **Antenna cavities and vias formation**: In this step the antenna cavities and BGA cavities are formed on the bottom side of the chip, and the vias needed for ground connection through the chip on the top side. This step is performed in multiple sub-steps:

    (a) **Contact lithography** is used on the bottom side of the sample to pattern the cavities and BGA cavities in a soft mask of photoresist on top of the hard mask, following the steps of appendix A.2.1 [40].

   (b) **Frontside protection**. This step is needed because the hard mask on the frontside could be affected when performing the dry etching step on the backside. Apply a bit of AZ5214E[63] resist using a cotton swab, on the backside of the sample. Make sure the whole surface is covered. Bake the sample on 100° for 3 minutes.

   (c) **Dry etching** of the hard mask is done to transfer the cavities pattern from the soft mask to the hard mask, following the steps of appendix A.2.2 [40].

   (d) Repeat steps (a) to (c) to imprint the vias of the frontside into the hard mask. To align the vias with the cavities on the backside, alignment vernier markers are provided in the lithography maskers. Backside alignment is specified in appendix A.1.

   (e) **Resist removal**. This step removes the resist that is applied in step (c) for protection. Place the sample in a ultrasonic bath filled with acetone $(CH_3)_2CO)$ for about 30 seconds.

   (f) **Wet etching** using KOH as etchant. Precise steps are explained in Appendix A.2.3 [40]. This etchant has the characteristic that the etch rate differs strongly for different lattice planes. The etch rate in the 100 planes is about 300 times faster than in the 111 planes [64]. A typical etch rate in the $< 100 >$ directions is 1:25 µm/min. Because the silicon substrate has a $< 100 >$ orientation this an-isotropic etch will yield a cavity bottom along the (100) plane, but sidewalls along the 111 planes under an angle of 54,74° ($\tan^{-1}(\sqrt{2})$) with the surface. This self limiting etch can be used to create vias. This will be the longest step as it takes 293 minutes to create the 440 µm depth cavities.

   (g) **Hard mask removal**. Removing the hard mask using hydrogen fluoride (HF) as a solvent. Please note that upon contact with moisture, including tissue, hydrogen fluoride immediately converts to hydrofluoric acid, which is highly corrosive and toxic. Only trained people may perform this step.

3. **Gold deposition**: This step is performed side by side and in two stages. First, a layer of 10 nm titanium (Ti) is sputtered on the sample. This will help for the adhesive of the gold. Secondly, a 1 nm gold (Au) layer is sputtered. As a check before continuing, electrical connection can be confirmed from the frontside to the backside.

4. **Microstrip line and aperture formation**: This processing step is similar to the cavities and vias formation step, except lithography is now performed in a regular way instead of using image reversal. This step is processed side by side and using following steps:
    (a) **Contact lithography**: First, the apertures are patterned in a photoresist layer on top of the gold layer on the backside of the sample. This is described in Appendix A.3.2 [40]. Frontside alignment can be used here. Because during etching of the cavities and vias also vernier markers are imprinted in the sample, and the masks for aperture and microstrip line lithography contains the positive or negative image of these vernier markers.
    (b) **Frontside protection** by using the same technique in the backside protection step during cavities and vias formation. Make sure the edges of the sample are also covered with resist, since there are edge connections present on the side.
    (c) **Wet etching** of the gold layer using potassium iodide (KI) and iodine as etchant. Procedure following Appendix A.3.3 [40].
    (d) repeat (a) to (c) now for the frontside to create the microstrip lines. Now protect the backside in step (b).

    Note that lithography on both sides uses a positive resist. But on the frontside we want to keep the gold layer to form the microstrip line and on the backside we want to erase the gold to form the apertures. Therefore, the mask defined for the apertures is a negative image.

5. **BCB layer creation**: A final layer is placed on the backside of the chip. This layer is made out of 10 nm thick BCB and has a pattern of openings in it that matches the BGA cavities. The precise process is explained in Appendix A.2. This layer will function as a solder mask to keep the BGA balls in place during soldering to the chip.

6. **BGA soldering**: The next step is to solder the BGA balls to the chip, by placing the balls into place and submit the chip to a reflow process.

7. **Attachment of the photoreceiver**: The LNA and PD of the photoreceiver are glued into place. Also the decoupling capacitors are glued next to the photoreceiver. Note a

conductive glue is needed as the photoreceiver and decoupling capacitors need a ground connection through the bottom side.

8. **Wire bonding**: All components needed to be interconnected. Wire bonding is used to connect the PD to the LNA of the photoreceiver and the output of the LNA to the microstrip line. Also the DC-feed lines are wire bonded to the decoupling capacitors and these to the DC biasing pads on the LNA.

9. **Pigtailing the fibers**: The input optical fibers are attached to the antenna array using the provided Plexiglas mount. The end of the fibers are then pig tailed.

Chapter 5

Measurements

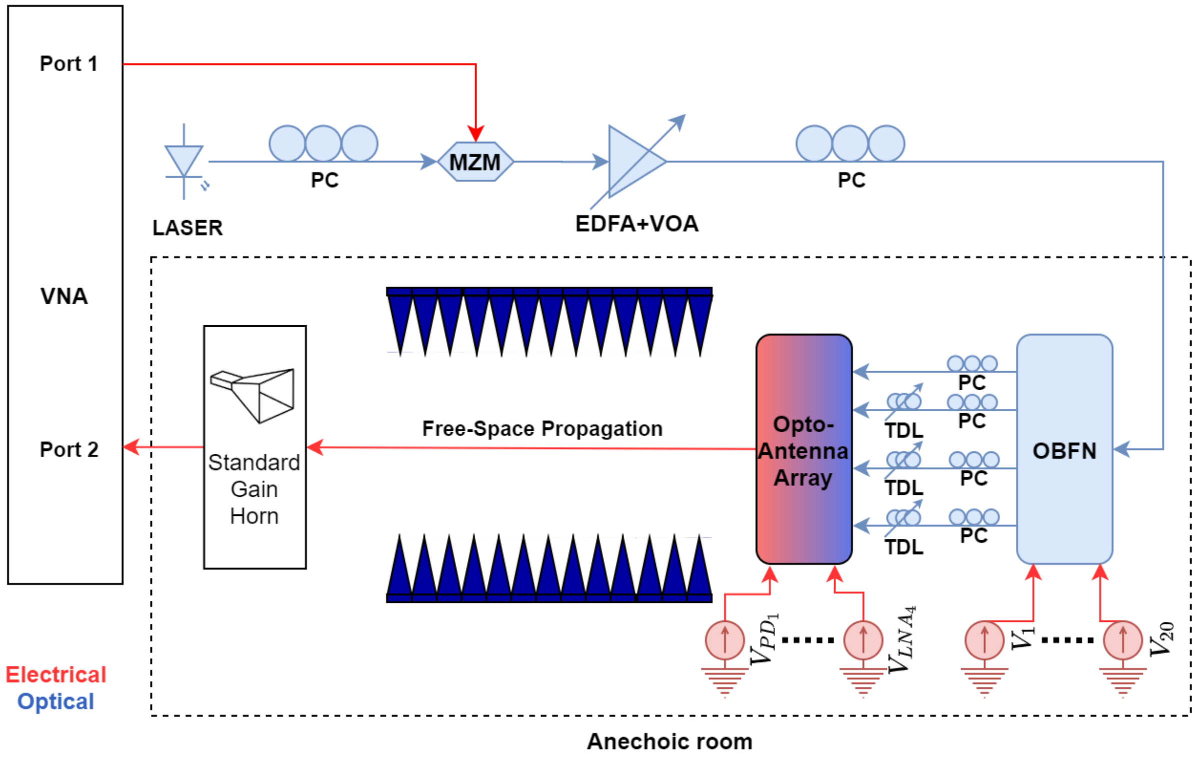
In this chapter, normally, validation of the total system performance should be elaborated. Unfortunately, due to the Covid-19 outbreak, the actual measurements couldn't be performed. Nevertheless, section 5.1 accurately describes the most interesting measurement setups to validate the total system. In section 5.2, the discussion of the measurement results is substituted by a sensitivity analysis on fabrication errors that can occur during processing.

5.1 Setup

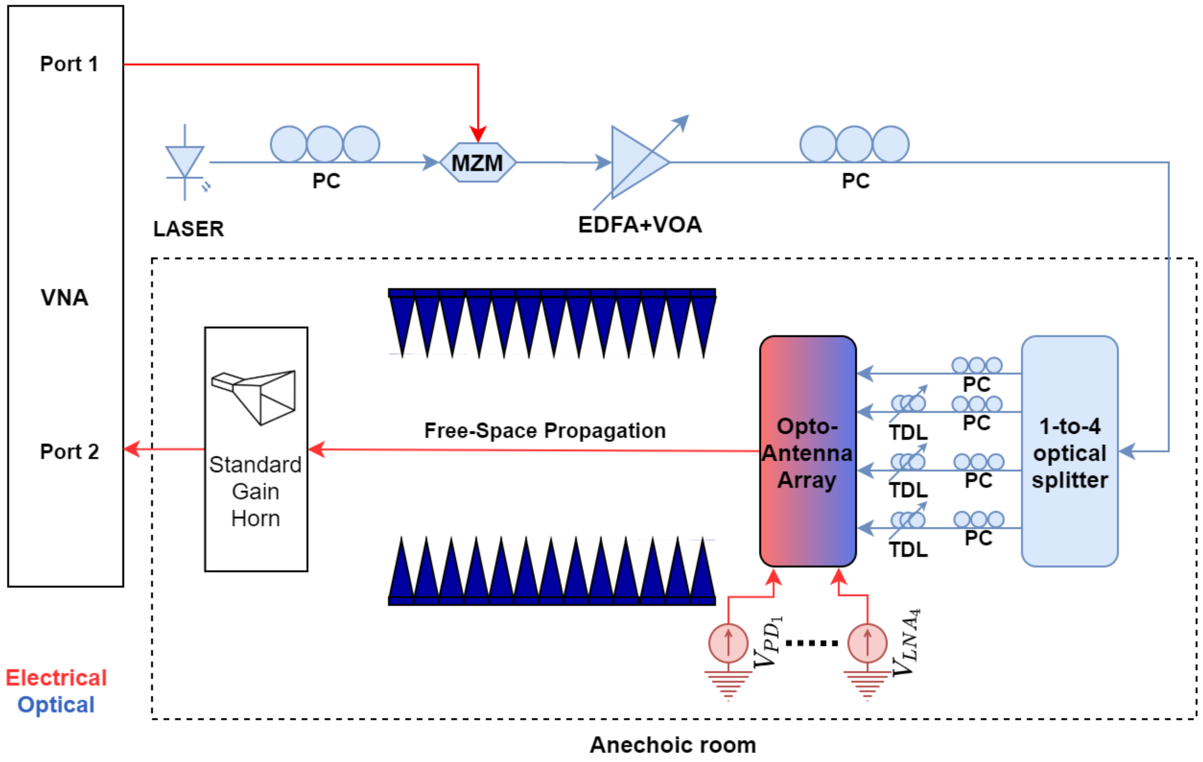
In this section two possible measurements setups are presented. The first one can be used to measure the radiation pattern of the antenna array and validate the beam steering capabilities by using the gain comparison method and is schematically shown in Fig. 5.1. The other setup can be used to measure the link performance of the total system. This is shown in Fig. 5.2.

First of all, validation of the active opto-electric phased array with optical beamforming is performed by measuring the far-field radiation pattern in free-space conditions. Fig. 5.1 is a schematic of the measurement setup. Measurement is done by using a vector network analyzer (VNA), of which one port is used to external modulate an optical signal generated by a continuous wave laser using a quadrature biased Mach-Zehnder modulator (MZM). The emitted light is coupled into a standard single mode fiber (SSMF) and passes through a polarization controller (PC). The power of the optical signal entering the fiber is controlled using a cascade of an erbium doped fiber amplifier (EDFA) and variable optical attenuator (VOA). The SSMF is routed into the anechoic room and is spliced to the input fiber of the OBFN, which is pigtailed. The OBFN is also connected to 20 voltage sources to control the time delay. These voltages are supplied by a dedicated board with a micro-controller and 20 digital to analog converters (DACs), as illustrated in Fig. 5.1a. The 4 optical signals coming from the OBFN are connected to the antenna array with PCs and tunable delay lines (TDLs) in between. These TDLs are needed to calibrate out the difference in fiber length between OBFN and antenna array. This connection is also done by splicing the fibers from the antenna array to the fiber at the output of the TDL. Power supplies are also attached to the antenna array by using the provided pin-header to feed the photoreceivers. Each photoreceiver needs a supply to bias the PD and feed the LNA, so 8 power supplies are needed. The antenna array is mounted on an antenna positioning system.

In the far-field of the antenna array a standard gain horn antenna is placed. The output of this antenna is connected to the second port of the VNA. Using the gain comparison method the radiation pattern of the antenna array can be evaluated. This setup is based on the realization of a passive opto-antenna as downlink RAU for RFoF by Olivier Caytan [65]. One could measure in a simpler way by substituting the OBFN by a 1-to-4 optical splitter, as depicted in Fig. 5.1b. Hereby, the performance of the antenna array alone can be validated and by adjusting the TDL the OBFN can be mimicked. The far-field radiation pattern can be measured for several frequencies and angles. Note that the used laser, MZM and SSMF should be characterized first to be calibrated out of the measurements. From the radiation pattern the realized gain, front-to-back ratio, beamwidth, side lobe level and maximum achievable steer angle can be extruded.



(a) Total system setup



(b) Simple measurement setup

Figure 5.1: Schematic representation of the measurement setup

In a next step, a data link is set up, as shown in Fig. 5.2. This results in a full link. The setup is largely identical to the previous measurement setup. An arbitrary waveform generator (AWG) is used here to modulate the optical carrier using a MZM. However, the output of the standard gain horn is now applied to a real time oscilloscope (RTO), if needed down-conversion can be applied before coupling to the RTO. From the RTO the root-mean-square Error Vector Magnitude (rms-EVM) or other data link parameters can be read. This is based on the measurement setup used in validating the photoreceiver [43].

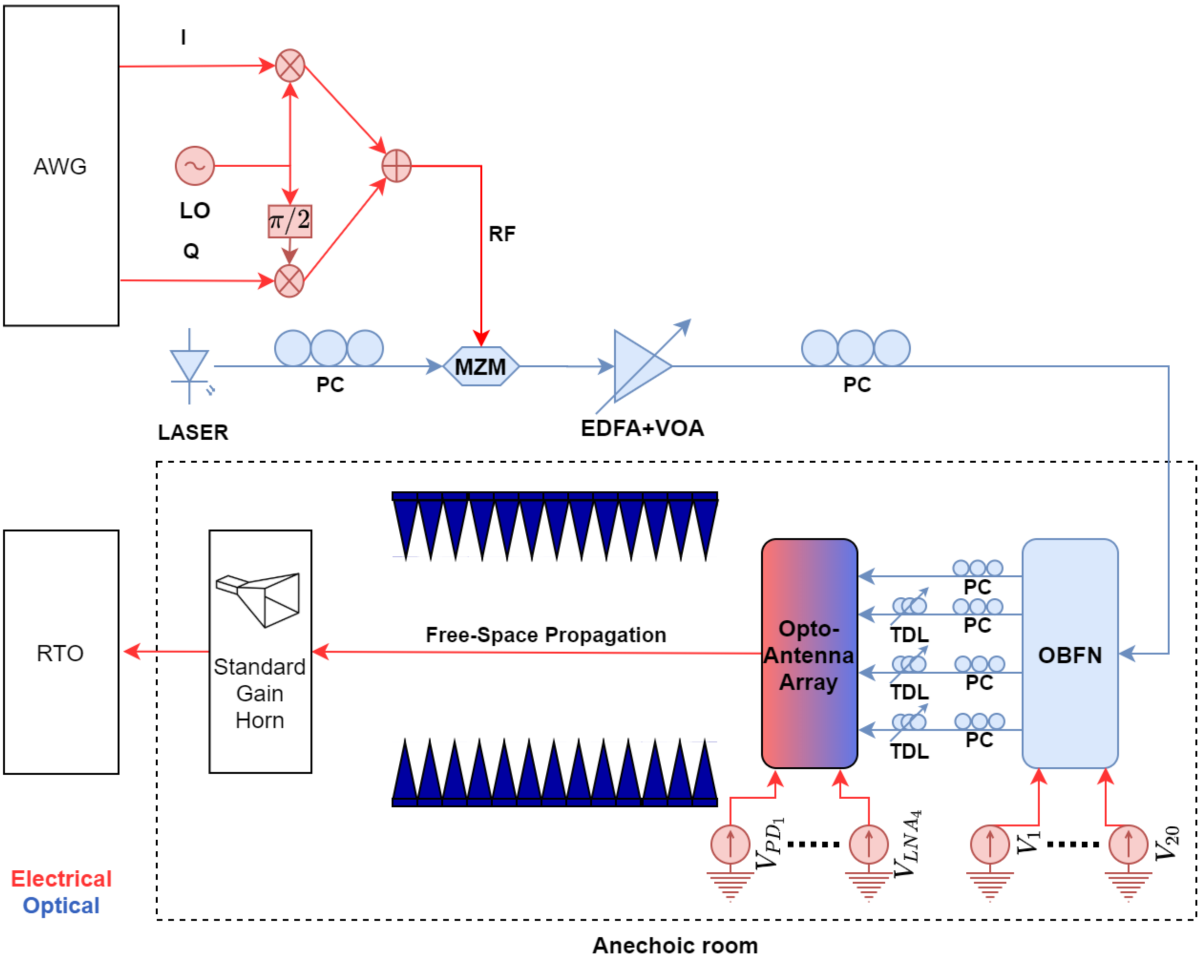


Figure 5.2: Schematic representation of a data link setup

5.2 Sensitivity analysis

Because no measurements could be executed, the discussion of the measurement results has been substituted by a sensitivity analysis. This sensitivity analysis examines the influence of fabrication errors on the passive S-parameters of the antenna array. Only the $|S_{11}|$ scattering parameter is considered due to the symmetry of the antenna array, as this is similar to $|S_{22}|$, $|S_{33}|$ and $|S_{44}|$.

5.2.1 Tolerances related to PCB manufacturing

First, the fabrication tolerances associated with PCB manufacturing are investigated [19], which result in errors on the patch size and/or misalignment of the patches. The size error is simulated as follows. The size of the patches are for both simultaneously increased and decreased in length and width by 1% up to max. 4%. The resulting $|S_{11}|$ parameter is plotted in Fig. 5.3. As the patch sizes change the resonance frequencies of the antenna change. This is logical because the dimensions of the patches determine the resonant frequencies. When the patches decrease more than 1% in size this results in S-parameters out of the desired frequency band. An increase in size is tolerated up to 4%, to have the bandwidth in the desired frequency range.

In Fig. 5.4, the simulated $|S_{11}|$ parameter is plotted when the patches are misaligned in several ways. Misalignment is simulated by displacing the patches in the x- or y-direction by 250 or 500 µm, note the labels on the figures are wrong. In Fig. 5.4a and 5.4b both patches are displaced simultaneously in the x-direction and in the y-direction, respectively, resulting in both patches being misaligned with reference to the chip. As observed from the simulated S-parameters shown in Fig. 5.4a and 5.4b, displacement in the y-direction has a more severe effect than displacement in the x-direction, resulting in a significant decrease in bandwidth and increase in input reflection. This is in agreement with the analysis performed by Sullivan and Schaubert [66] on aperture coupled patch antennas and Pozar's simple model for aperture coupled microstrip antennas [67]. Since the cavity fields are independent of x, the aperture may be located any-

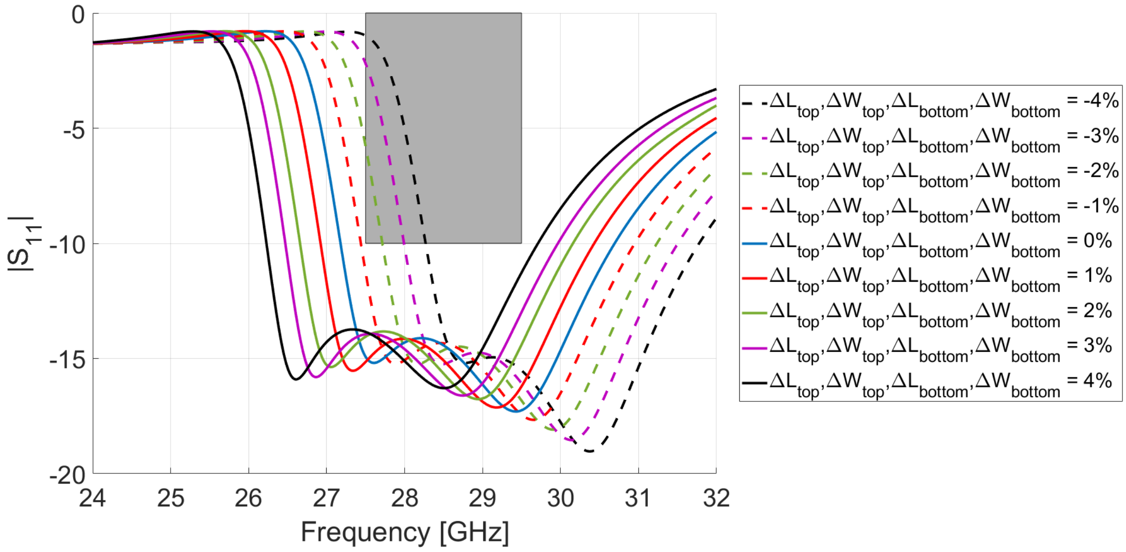
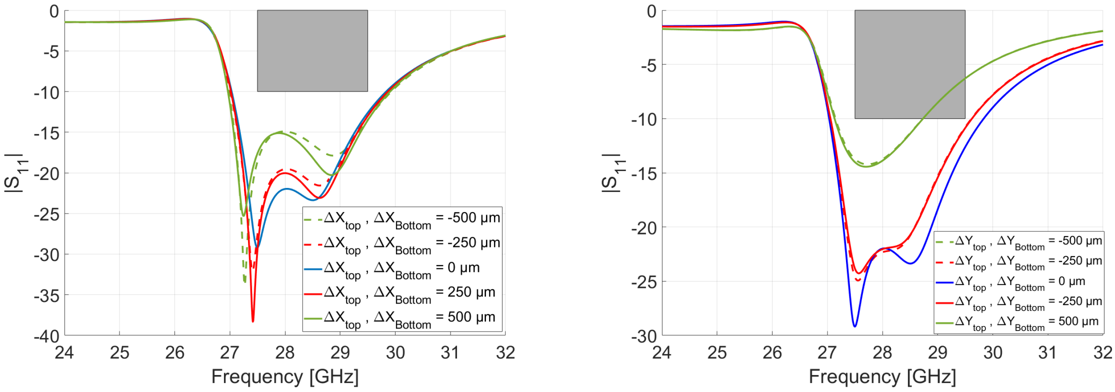


Figure 5.3: Simulated S-parameter of the antenna array for varying patch sizes

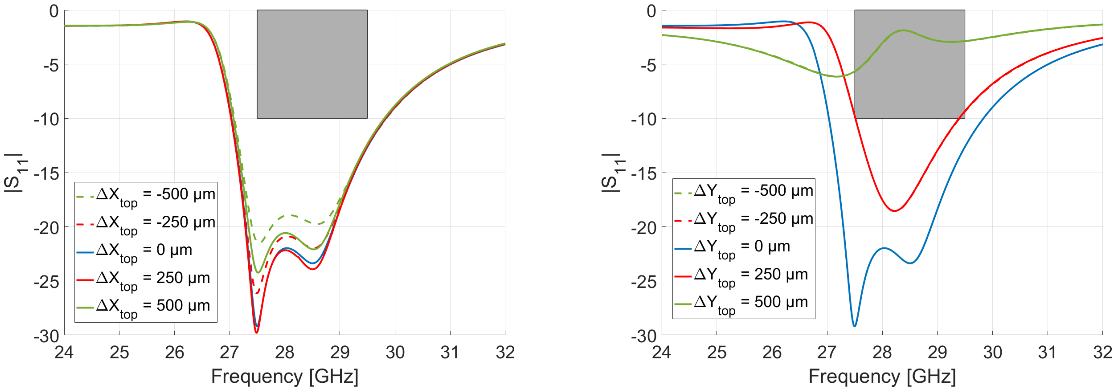
where along a line with constant y value, without having a great influence on the coupling factor between aperture and patches [67].

When only one patch is misaligned in the y-direction (Fig. 5.4d and Fig. 5.4f), the antenna array input return loss is increased a lot more compared when both patches are misaligned (Fig. 5.4b). When the patches are misaligned with reference to each other the coupling between them changes significantly. A change in the upper patch position affects the fringing fields of the bottom patch, then the effective length of both patches must also change and, obviously, this change in the effective length moves the antenna's resonant frequencies [68]. Concluded is that a displacement in the y-direction decreases the bandwidth of the antenna and increases reflection



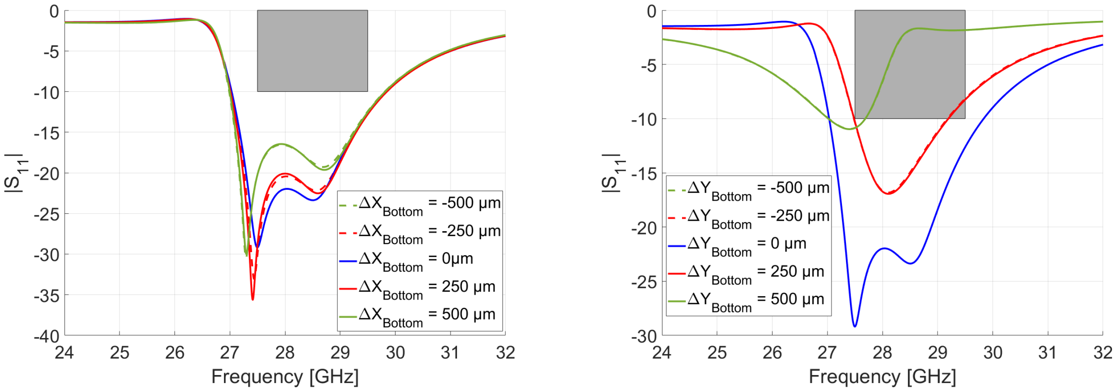
(a) $|S_{11}|$ parameter for patches moved in x direction simultaneously

(b) $|S_{11}|$ parameter for patches moved in y direction simultaneously



(c) $|S_{11}|$ parameter for top patch moved in x direction

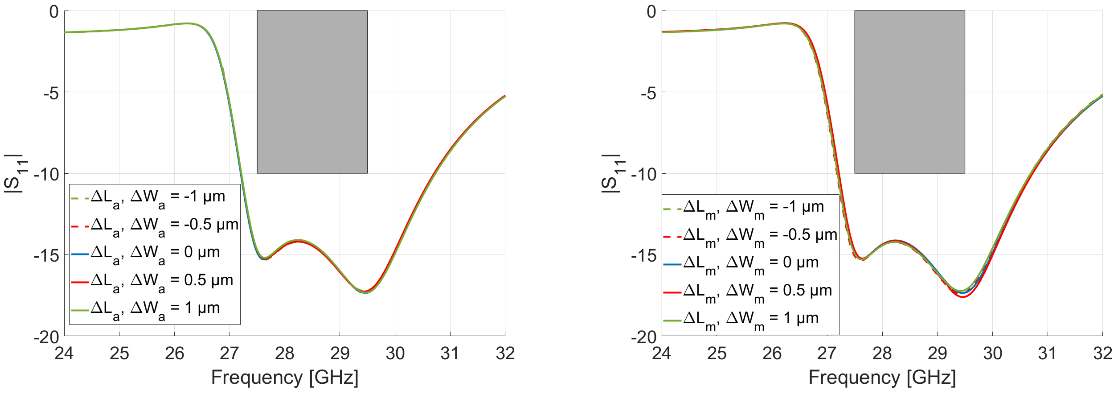
(d) $|S_{11}|$ parameter for top patch moved in y direction



(e) $|S_{11}|$ parameter for bottom patch moved in x direction

(f) $|S_{11}|$ parameter for bottom patch moved in y direction

Figure 5.4: Simulated $|S_{11}|$ parameter of the antenna array when patches are misaligned



(a) $|S_{11}|$ of the antenna array with varying aperture size

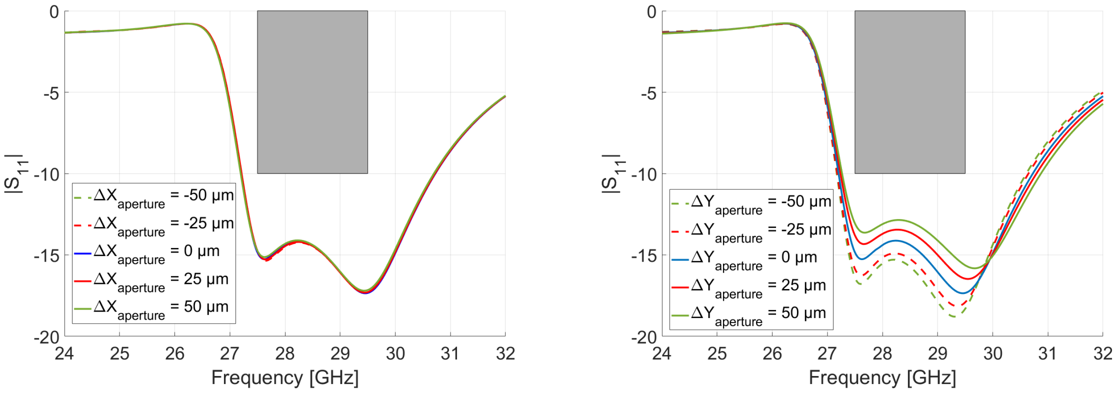
(b) $|S_{11}|$ of the antenna array with varying microstrip line size

Figure 5.5: Simulated S-parameters of the antenna array with varying aperture and microstrip line sizes

5.2.2 Tolerances related to chip fabrication

Secondly, the tolerances related to the fabrication of the chip are investigated. The error on feature size in CMOS technology, by using lithography is estimated to be 1 µm. This error is applied to the dimensions of the aperture and microstrip line, respectively, resulting in change in width and length of aperture and microstrip, respectively. The resulting $|S_{11}|$ is plotted in Fig. 5.5. Based on Fig. 5.5a, it can be concluded that the fabrication error has no or little influence on the reflection coefficient of the antenna array. From Fig. 5.5b allows similar conclusions about the microstrip line size.

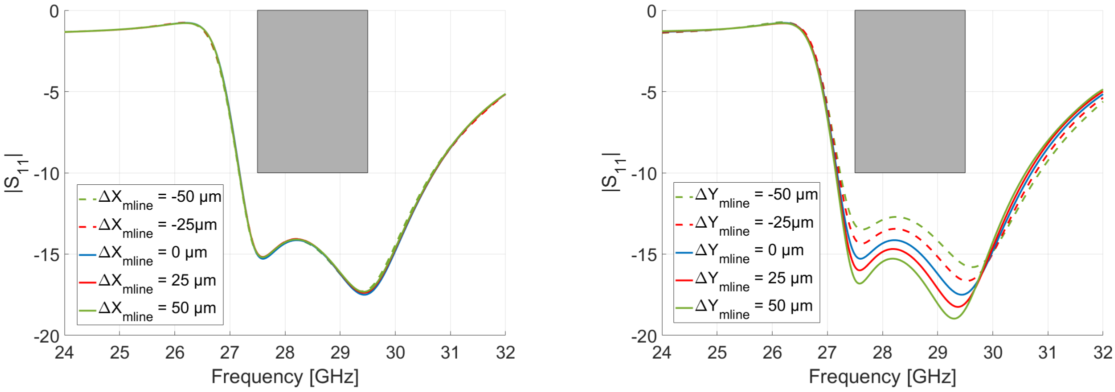
Next, misalignment during lithography is investigated. This can result in the aperture or the microstrip line to be misaligned with respect to the stacked patches and antenna cavities. Misalignment of the vias is assumed to be negligible. Simulation is performed by shifting the aperture and microstrip line by 25 µm and 50 µm in both ±x- and ±y-direction. In Fig. 5.6 the simulation results of misalignment of the aperture are shown and Fig. 5.7 shows misalignment of the microstrip line. For both the aperture and microstrip feeding line there is no or little influence on the reflection coefficients due to a displacement in the x-direction.



(a) $|S_{11}|$ when aperture is moved in x-direction (b) $|S_{11}|$ when aperture is moved in y-direction

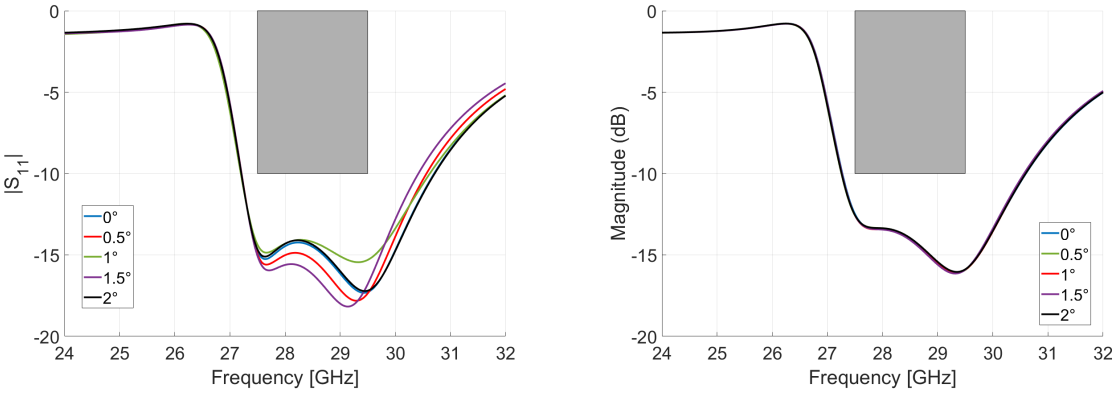
Figure 5.6: Simulated S-parameters of the antenna array with aperture misaligned

In contrast, the displacement in the y-direction has a significant influence on the reflection coefficients. In particular, if the microstrip line is moved in the y-direction the stub length of the microstrip line changes, which is the length of the microstrip going beyond the center of the aperture. As the stub length tunes the excess reactance of the aperture coupled antenna [66], this influences the input impedance of the antenna elements.



(a) $|S_{11}|$ when microstrip line is moved in x-direction (b) $|S_{11}|$ when microstrip line is moved in y-direction

Figure 5.7: Simulated S-parameters of the antenna array with microstrip line misaligned



(a) $|S_{11}|$ parameter when chip is rotated

(b) $|S_{22}|$ parameter when chip is rotated

Figure 5.8: Simulated S-parameters of the antenna array when the chip is rotated compared to the PCB

5.2.3 Tolerances related to PCB/chip alignment

Finally, when the PCB and chip are assembled, misalignment can occur. This misalignment can occur between them in the x- or y-direction, as already discussed for the stacked patches, but also by placing the chip slightly rotated on the PCB. Simulation of this rotation is performed by rotating the chip around its center by 0.5° up to 2°. Results from this simulation are shown in Fig. 5.8. Here a significant difference between the $|S_{11}|$ and $|S_{22}|$ parameter can be observed. As the patches are aligned in a row and a rotation of this row around its center has as result that patches undergo a rotation and displacement. This is more severe for the outer patches as these are placed further away from the center. The effect of rotation on the $|S_{22}|$ is concluded to be negligible, while the $|S_{11}|$ is only slightly affected, with the return loss remaining above -14 dB in the entire frequency band of interest.

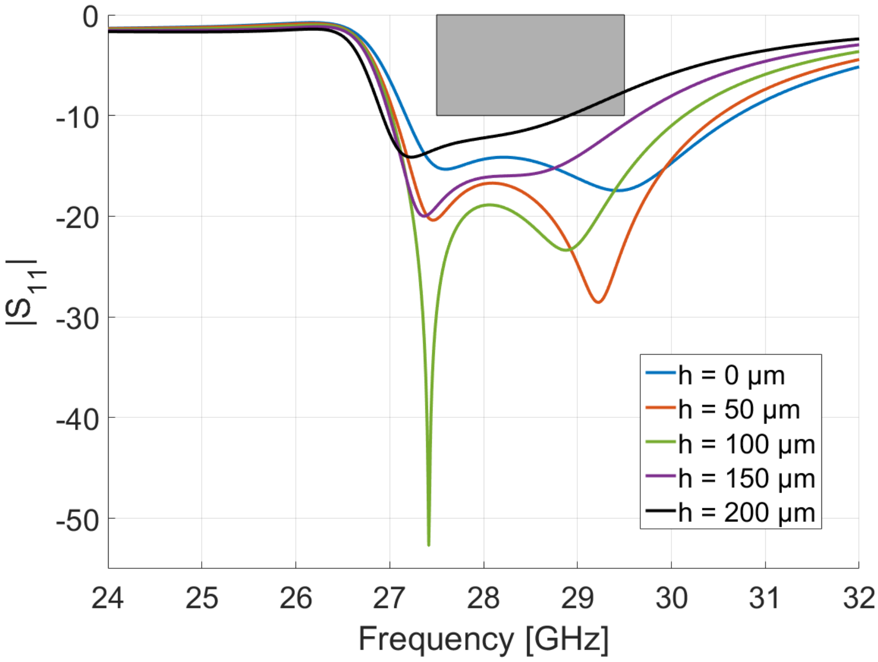


Figure 5.9: Simulated S-parameters of the antenna array when the height between chip and the PCB is varied

As a final analysis, variation of the diameter of the BGA balls is simulated, by changing the distance (h) between chip and PCB ranging from 0 µm to 200 µm in steps of 50 µm. This variation of the distance results in an air gap between PCB and chip. The resulting $|S_{11}|$ is shown in Fig. 5.9. it is observed that the bandwidth decreases if the distance between PCB and chip is increased. The required bandwidth is still achieved up to a distance of 150 µm. As the height between the PCB and chip increases, the cavity height increases, which impacts the coupling between aperture and patches and changes the input impedance of the antenna elements.

Chapter 6

Conclusion and future work

In this thesis, an active opto-electronic on-chip antenna array operating in the [27.5-29.5] GHz band was designed for use in next-generation communication systems.

First, an appropriate photoreceiver was selected that implements the opto-electronic conversion and amplification. The photoreceiver consists of a Ge-on-Si waveguide-integrated vertical p-i-n PD and a GaAs LNA [43]. This photoreceiver offers an external conversion gain of 224 V/W.

Secondly, a hybrid on-chip/PCB antenna array was designed, based on the compact, broadband and efficient antenna element proposed in [53]. This antenna element is optimized for integration with the photoreceiver. Full-wave simulations predict that the resulting antenna element has a broadside realized gain of 6.83 dBi in both the E- and H-planes, an impedance bandwidth of 3.61 GHz (ranging from 27.22 to 30.84 GHz) and exhibits a total efficiency over 90% at 28.5 GHz. A beamwidth of 79.9° and 87.1° are obtained in the E-plane and H-plane, respectively.

For deployment of the antenna element in a four-element ULA, several design decisions have been taken. First, the orientation of the antenna elements was considered. A 1-by-4 configuration was chosen as this allows for an easier way to couple the input optical fibers and provide the voltage supply for the photoreceiver. Secondly, the distance between the antenna elements was carefully optimized, as this distance results in a trade-off between mutual coupling, grating lobe suppression and structural stability. An inter-element spacing of $0.6{\cdot}\lambda_{min} = 6.10$ mm, with λ_{min} being the free-space wavelength at 29.5 GHz was chosen.

A simulation of the antenna array is performed to assess its performance. When the main beam is steered broadside, the antenna array has a bandwidth of 3.34 GHz, ranging from 27.27 to 30.61 GHz, a broadside realized gain of 12.4 dBi and a beamwidth of 21°. When the main beam is steered to 60°, the realized gain drops by 3.46 dB and the beamwidth increases to 25°. The relative side lobe level limits the scan range of the antenna array, resulting in a scan range of [-40°, 40°]. Within this range the relative side lobe level stays below -10 dB.

In combination with the OBFN, the full opto-electronic transmit antenna array system is obtained. As this OBFN is based on TTD, squint-free beam steering of the antenna array is guaranteed.

The immediate next steps are the fabrication and the validation of the designed antenna array. To this end, several measurement setups are proposed. From these measurements, the radiation pattern can be verified, while the main beam is steered in several directions. Furthermore, a high data-rate mmWave communication link can be set up using the proposed optically fed antenna array as transmitter. The proposed 1-by-4 array could also be extended to a 4-by-4 array although this would require a significant rerouting of the interconnection between the antenna elements and the photoreceiver. Finally, the proposed antenna array could be scaled to operate at even higher frequencies, e.g. at 60 GHz.

Appendix A

Clean room procedures

This is a extension to the Appendix A in the thesis of Dennis Maes [40]. In section A.1 explains how backside alignment can be performed during contact lithography. Section A.2 clarifies how a BCB layer can be formed on a silicon wafer.

A.1 Backside alignment

Backside alignment is used to align features on a lithography mask that will be transferred to the top side of a sample, to features on the backside of the same sample. Alignment is performed using following steps:

1. Position backside microscope to have a clear view of mask and sample.
2. Load mask without sample.
3. Grab image, by pressing the 'Grab image' function button.
4. Load sample (take care to position sample such that it is almost aligned).
5. Perform alignment, by aligning the image to the visible features on the backside of the sample through the microscope.

6. Expose the sample to the UV light with the desired expose time.

A.2 BCB layer formation

This section elaborates on placing a BCB layer on top of the sample and how to transfer a pattern into it. This is performed using following steps:

1. First step is to apply the BCB layer.
    (a) **BCB spincoaten**: A layer of BCB 3022-57 is spin coated on the sample. First 5 seconds at 500 rpm with acl 1, and then for 40 seconds at 1600 rpm at acl 10.
    (b) **BCB curing**: Place the samples on pre-heated hotplates of 150°C. Immediately raise the temperature for the hotplate to 180°C and bake for 30 minutes.
2. SiNx is applied on top of the BCB layer as a hard mask during etching.
3. Perform contact lithography with the solder mask masker by process described in Appendix A.2.1 [40]. This will create a soft mask with the pattern into it on the sample.
4. Dry etch the hard mask SiNx. Using the same technique as in Appendix A.2.2 [40].
5. Dry etch the BCB layer using a gas mixture involving CF4/O2 and SF6/O2 for 40 minutes [69].

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